



Complementary transistor pair in a single package

Datasheet — production data

Features

- Low V_{CE(sat)}
- Simplified circuit design
- Reduced component count
- Low spread of dynamic parameters

Application

■ Compact fluorescent lamp (CFL) 220 V mains

Description

The STD815CP40 is a hybrid complementary pair of power bipolar transistors manufactured by using the high voltage multi-epitaxial planar technology for high switching speeds and medium voltage capability.

The STD815CP40 is housed in dual island DIP-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in a new solution for compact fluorescent lamp (CFL).

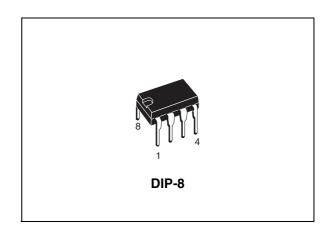


Figure 1. Internal schematic diagram

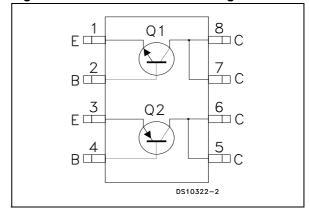


Table 1. Device summary

Order code	Marking	Package	Packing
STD815CP40	D815CP40	DIP-8	Tube

Electrical ratings STD815CP40

1 Electrical ratings

Table 2. Absolute maximum ratings

Cumbal	Dougnator	Value		Unit	
Symbol	Parameter	NPN	PNP	Oill	
V _{CBO}	Collector-base voltage (I _E = 0)	700	500	V	
V _{CEO}	Collector-emitter voltage (I _B = 0) 400		00	V	
V _{EBO}	Emitter-base voltage ($I_C = 0$, $I_B = 0.75$ A, $t_p < 10$ ms)		V _{(BR)EBO}		
I _C	Collector current		1.5		
I _{CM}	Collector peak current (t _P < 5 ms)	3		Α	
I _B	Base current		0.75		
I _{BM}	Base peak current (t _P < 1 ms)	1.5		Α	
P _{TOT}	Total dissipation at T _{amb} = 25 °C single transistor		2.6		
P _{TOT}	Total dissipation at T _{case} = 25 °C single transistor		45		
T _{STG}	Storage temperature		- 65 to 150		
TJ	Max. operating junction temperature	150		°C	

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA} (1)	Thermal resistance junction-ambient (single transistor)	48	°C/W
R _{thJC} (1)	Thermal resistance junction-case (single transistor)	2.7	°C/W

^{1.} When mounted on 25mm square pad of 2 oz. copper, $t \le 10$ sec.

Note: For PNP types voltage and current values are negative.

2 Electrical characteristics

 $T_{case} = 25$ °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{CES}	Collector cut-off current (V _{BE} = 0)	For NPN: V _{CE} = 700 V V _{CE} = 700 V For PNP: V _{CE} = 500 V			1 5	mA mA
V _{(BR)EBO}	Emitter-base breakdown voltage (I _C = 0)	$V_{CE} = 500 \text{ V}$ $T_{C} = 125^{\circ}\text{C}$ $I_{E} = 10 \text{ mA}$ For NPN: For PNP:	12 5		18 10	WA V V
V _{CEO(sus)} ⁽¹⁾	Collector-emitter sustaining voltage (I _B = 0)	I _C = 5 mA	400			V
V _{CE(sat)} ⁽¹⁾	Collector-emitter saturation voltage	$I_C = 0.5 \text{ A}$ $I_B = 0.1 \text{ A}$ $I_C = 0.35 \text{ A}$ $I_B = 50 \text{ mA}$			0.5 1	V V
V _{BE(sat)} ⁽¹⁾	Base-emitter saturation voltage	I _C = 0.5 A I _B = 0.1 A			1	V
h _{FE} ⁽¹⁾	DC current gain	$\begin{split} I_{C} &= 10 \text{ mA} & V_{CE} &= 5 \text{ V} \\ I_{C} &= 0.35 \text{A} & V_{CE} &= 5 \text{ V} \\ I_{C} &= 1 \text{ A} & V_{CE} &= 5 \text{ V} \end{split}$	16		34	
t _r t _s	Resistive load Rise time Storage time Fall time	$I_{C} = 0.35 \text{ A}$ $V_{CC} = 125 \text{ V}$ $I_{B1} = 70 \text{ mA}$ $I_{B2} = -70 \text{ mA}$ $t_{p} \ge 25 \mu\text{s}$		100 2.2 0.2		ns µs µs
t _s	Inductive load Storage time Fall time	$\begin{split} & I_{C} = 0.5 \text{ A} & I_{B1} = 0.1 \text{ A} \\ & V_{BE(off)} = -5 \text{ V} \\ & V_{clamp} = 300 \text{ V} & L = 10 \text{ mH} \end{split}$		450 80		ns ns

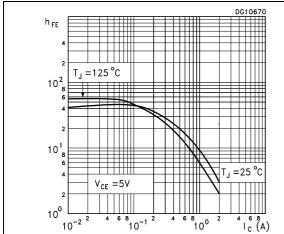
^{1.} Pulse test: pulse duration \leq 300 µs, duty cycle \leq 2 %.

Note: For PNP types voltage and current values are negative

Electrical characteristics STD815CP40

2.1 Electrical characteristics (curves)

Figure 2. DC current gain NPN ($V_{CE} = 5 \text{ V}$) Figure 3. DC current gain PNP ($V_{CE} = -5 \text{ V}$)



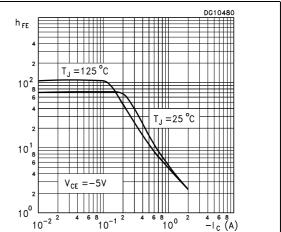
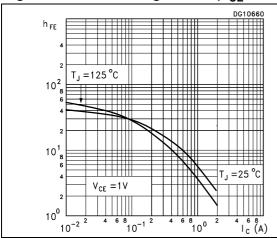


Figure 4. DC current gain NPN ($V_{CE} = 1 \text{ V}$) Figure 5. DC current gain PNP ($V_{CE} = -1 \text{ V}$)



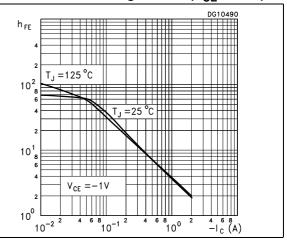


Figure 6. Derating curve

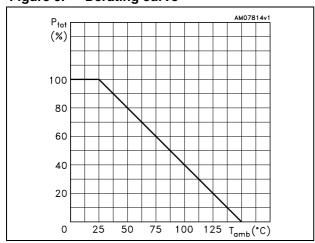
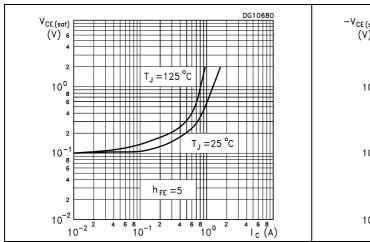


Figure 7. Collector emitter saturation voltage Figure 8. Collector emitter saturation voltage NPN PNP



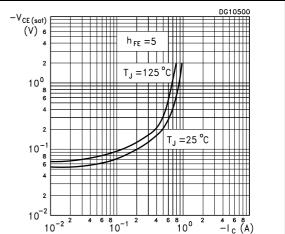
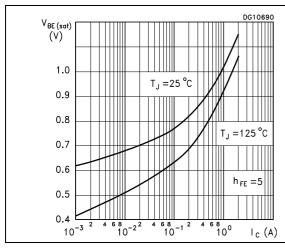


Figure 9. Base emitter saturation voltage NPN

Figure 10. Base emitter saturation voltage PNP



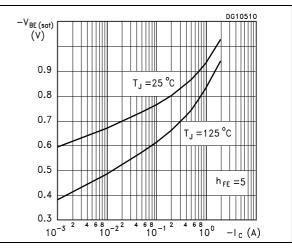
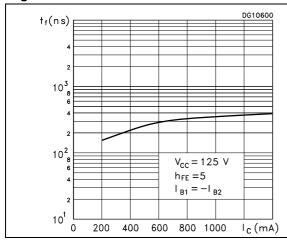
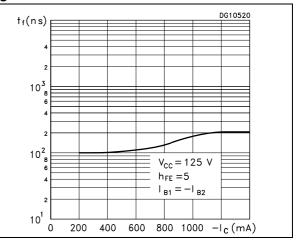


Figure 11. Resistive load fall time NPN

Figure 12. Resistive load fall time PNP

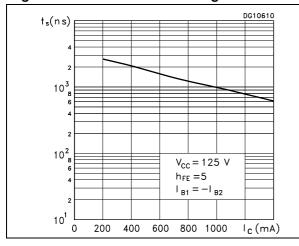




Electrical characteristics STD815CP40

Figure 13. Resistive load storage time NPN

Figure 14. Resistive load storage time PNP



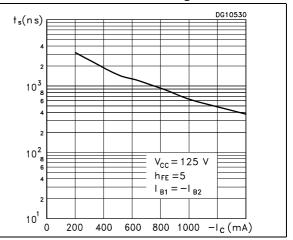
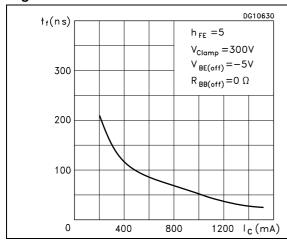


Figure 15. Inductive load fall time NPN

Figure 16. Inductive load fall time PNP



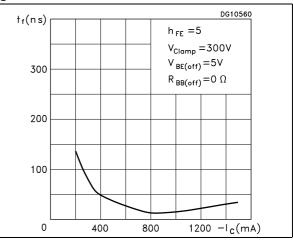
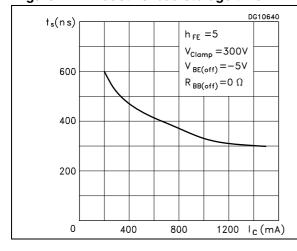


Figure 17. Inductive load storage time NPN

Figure 18. Inductive load storage time PNP



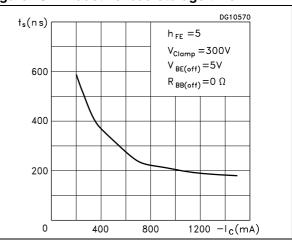
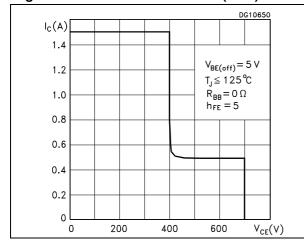
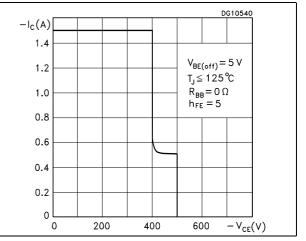


Figure 19. Reverse biased SOA (NPN)

Figure 20. Reverse biased SOA (PNP)





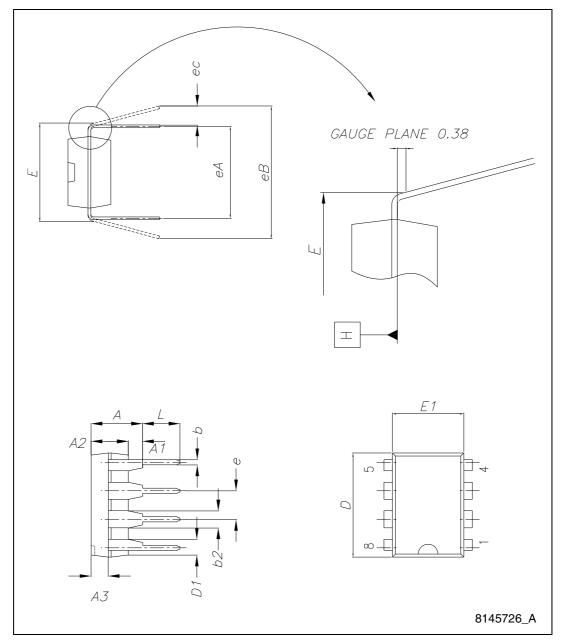
3 Package mechanical data

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Table 5. DIP-8 mechanical data

Dim.		mm.	
	Min.	Тур.	Max.
А			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
С	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
Е	7.62		8.25
E1	6.25		6.45
е		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

Figure 21. Drawing dimension DIP-8



Revision history STD815CP40

4 Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jun-2008	1	Initial release
26-May-2009	2	Updated mechanical data <i>Table 5 on page 8</i> and <i>Figure 21 on page 9</i> .
29-Jun-2010	3	Modified: Table 2 and Table 3 on page 2, added Section 2.1: Electrical characteristics (curves).
05-Oct-2012	4	Table 2 and Table 3 on page 2 have been modified.

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