EPC2106 – Enhancement-Mode GaN Power Transistor Half Bridge
Preliminary Specification Sheet

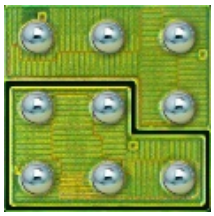
Status: Engineering

Features:

- V_{DS}, 100 V
- High Frequency Operation
  - High Density Footprint
- Low Inductance Package
- Pb-Free (RoHS Compliant), Halogen Free

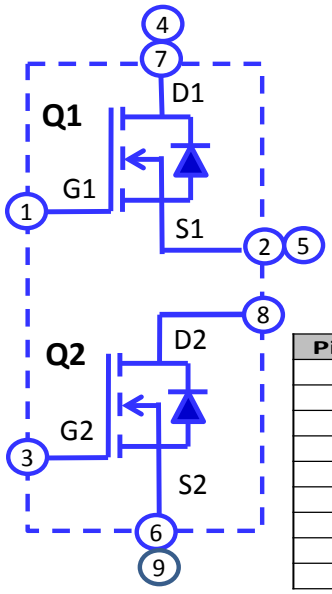
Applications:

- High Frequency DC-DC Conversion
- Class-D Audio



EPC2106 devices are supplied only in passivated die form with solder balls

Die Size: 1.35 mm x 1.35 mm



Pin No.	Description	Device
1	Gate	Q1
2	Source	Q1
3	Gate	Q2
4	Drain	Q1
5	Source	Q1
6	Source	Q2
7	Drain	Q1
8	Drain	Q2
9	Source	Q2

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage (V_{SW} to P_{GND}, V_{IN} to V_{SW})	100 V
Maximum Gate – Source Voltage Range (Gate 1 to V_{SW}, Gate 2 to P_{GND})	-4 V < V_{GS} < 6 V
Continuous Drain Current, 25 °C, $R_{\theta JA}$ = 350 °C/W	1.7 A
Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 µs	18 A
Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Voltage (BV_{DSS})	V_{GS} = 0 V, I_D = 300 µA	100 V
Maximum Drain – Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V	250 µA
Maximum $R_{DS(on)}$	V_{GS} = 5 V, I_D = 2 A	70 mΩ
Typical $R_{DS(on)}$	V_{GS} = 5 V, I_D = 2 A	55 mΩ
Gate – Source Threshold Voltage	I_D = 0.6 mA, V_{DS} = V_{GS}	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	1 mA
Gate – Source Maximum Negative Leakage	V_{GS} = -4 V	-250 µA

T_J = 25 °C unless otherwise stated

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value		
		Q1 Control FET	Q2 Sync FET	Unit
C_{ISS} (Input Capacitance)	V_{DS} = 50 V, V_{GS} = 0 V	75	79	pF
C_{OSS} (Output Capacitance)		42	56	
C_{RSS} (Reverse Transfer Capacitance)		0.9		
Q_G (Total Gate Charge)	V_{DS} = 50 V, I_D = 2 A, V_{GS} = 5 V	0.73	0.76	nC
Q_{GS} (Gate to Source Charge)	V_{DS} = 50 V, I_D = 2 A	0.22	0.24	
Q_{GD} (Gate to Drain Charge)		0.165		
$Q_{G(TH)}$ (Gate Charge at Threshold)		0.15	0.16	
Q_{OSS} (Output Charge)	V_{DS} = 50 V, V_{GS} = 0 V	3.4	4.4	
Q_{RR} (Source-Drain Recovery Charge)		0		

T_J = 25 °C unless otherwise stated

THERMAL CHARACTERISTICS

		TYPICAL		
		Q1 Control FET	Q2 Sync FET	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3		°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board (Note 2)	30	31	°C/W
$R_{\theta 12}$	Thermal Resistance, Cross-Coupling	29		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	81		°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
Note 2: ΔT is determined by the following matrix equation:

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 30 & 29 \\ 29 & 31 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

This matrix equation lets you calculate the temperature rise of each FET, given the power dissipated in each FET.
Thermal models for EPC devices available at http://epc-co.com/epc/DesignSupport/DeviceModels.aspx

Figure 1a: EPC2106-Q1 Typical Output Characteristics at 25°C

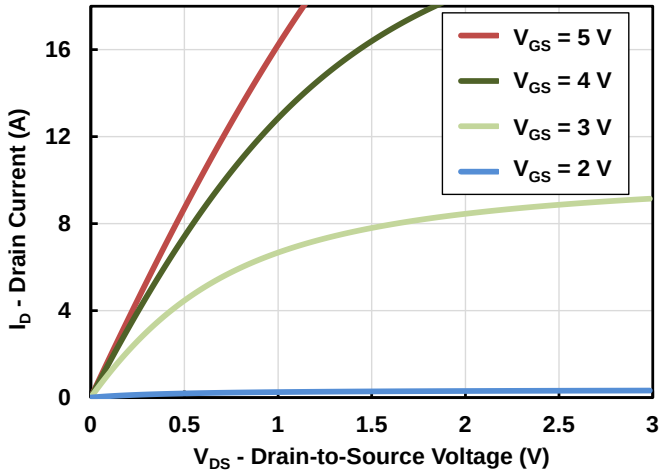


Figure 1b: EPC2106-Q2 Typical Output Characteristics at 25°C

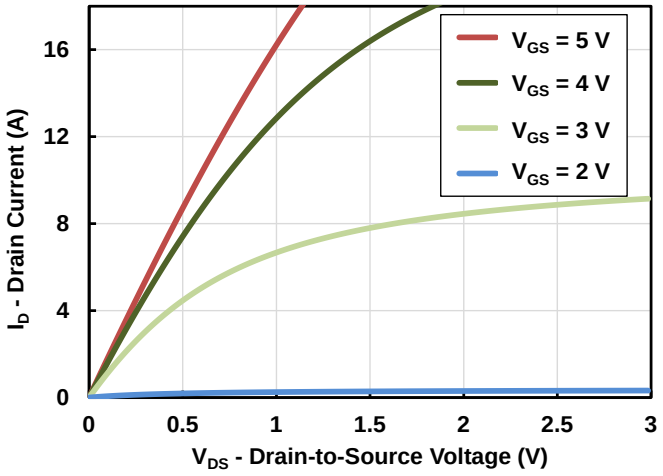


Figure 2a: EPC2106-Q1 Transfer Characteristics

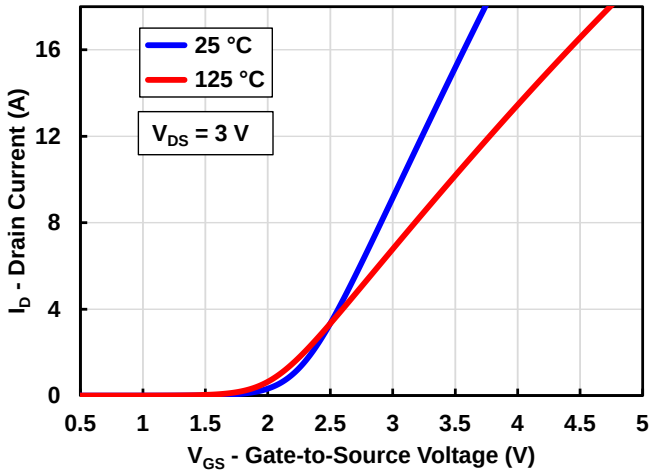


Figure 2b: EPC2106-Q2 Transfer Characteristic

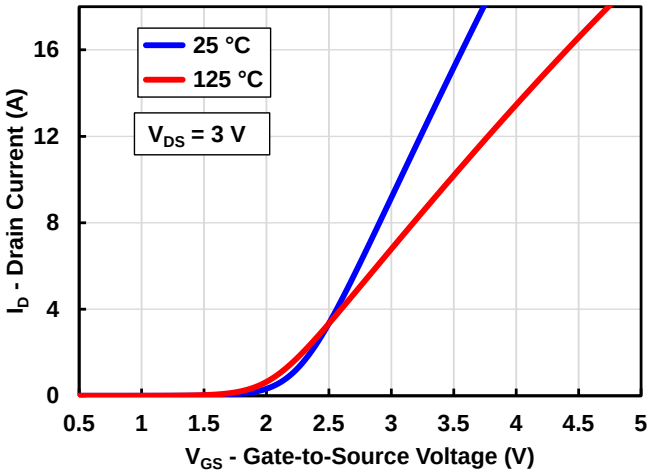


Figure 3a: EPC2106-Q1: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

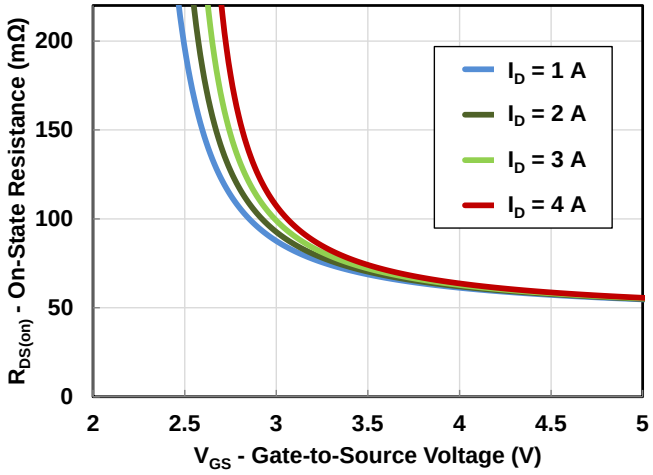


Figure 3b: EPC2106-Q2: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

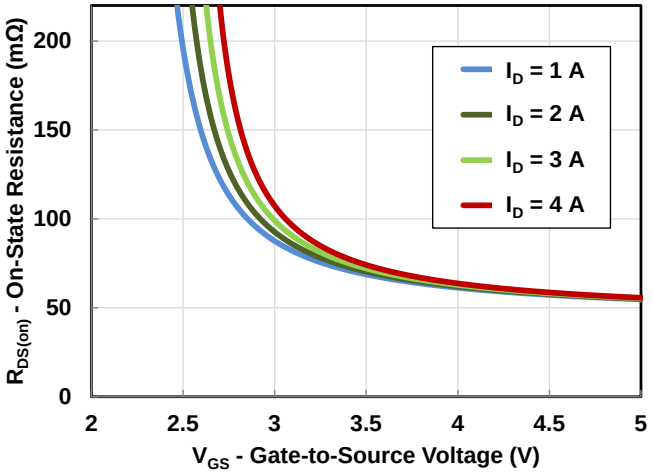


Figure 4a: EPC2106-Q1: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

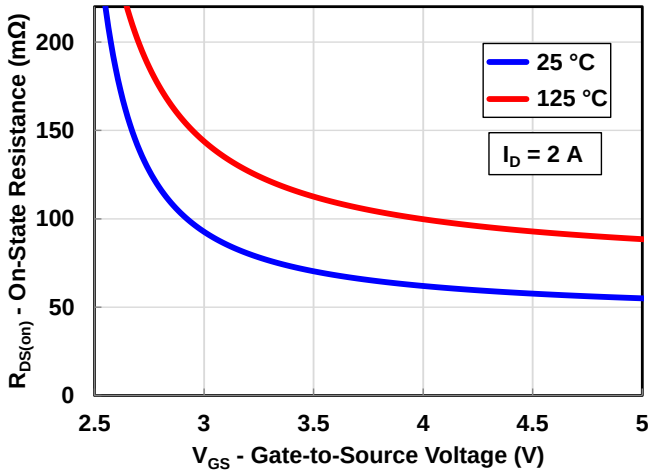


Figure 4b: EPC2106-Q2: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

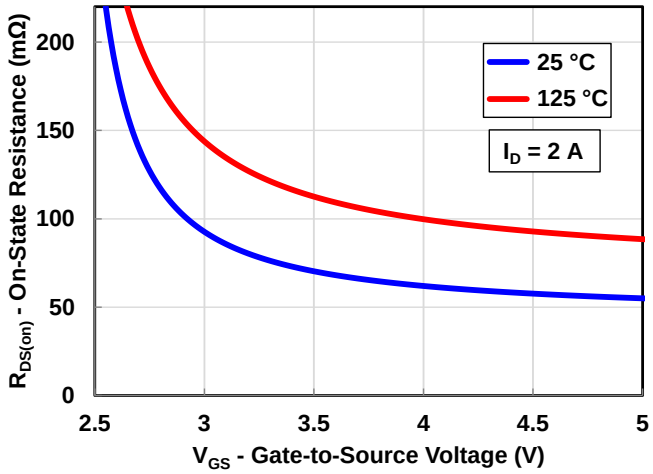


Figure 5a: EPC2106-Q1: Capacitance (Linear Scale)

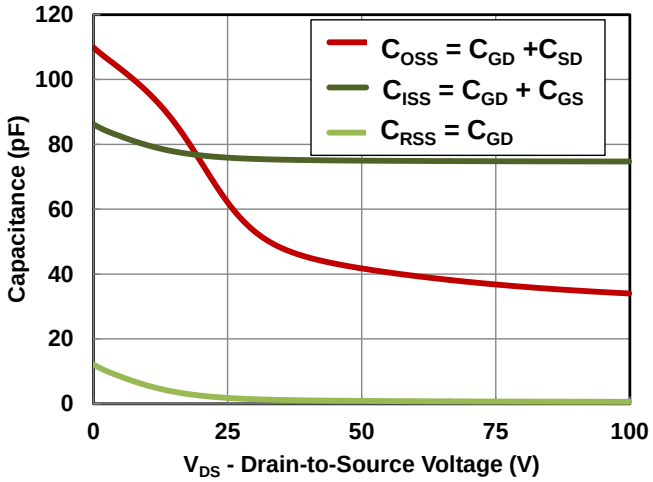


Figure 5b: EPC2106-Q2: Capacitance (Linear Scale)

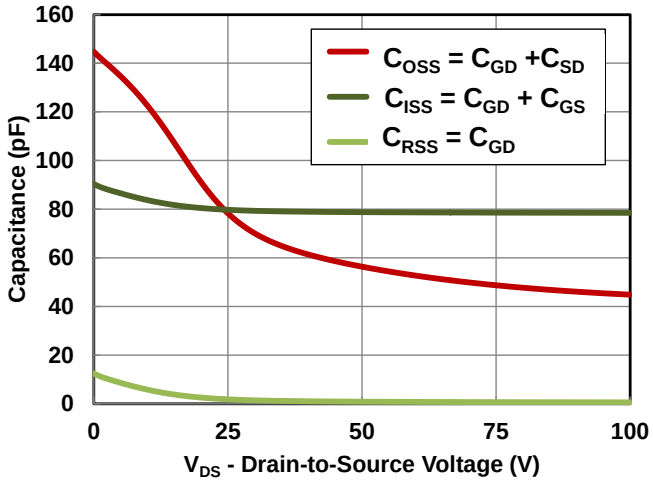


Figure 5c: EPC2106-Q1: Capacitance (Log Scale)

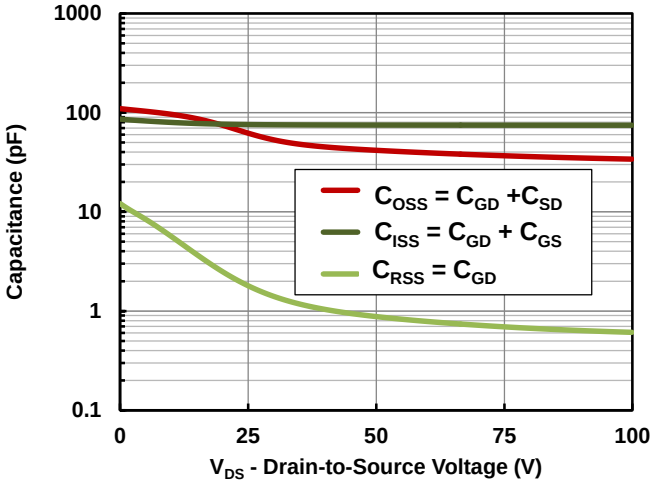


Figure 5d: EPC2106-Q2: Capacitance (Log Scale)

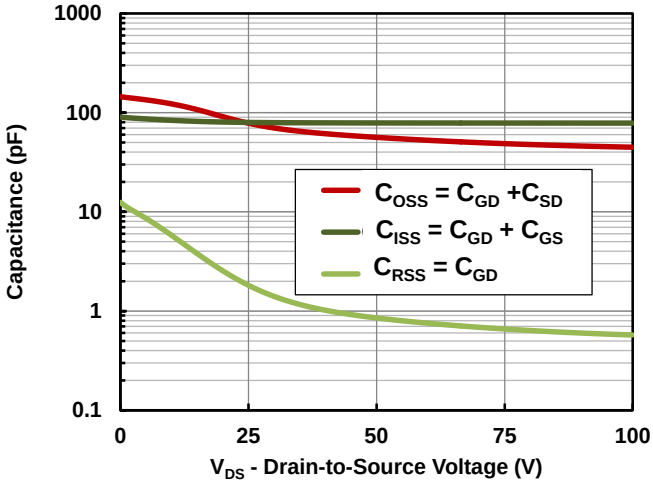


Figure 6a: EPC2106-Q1: Gate Charge

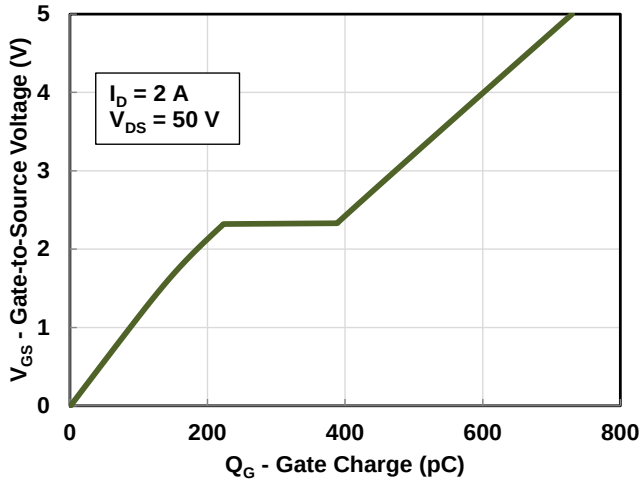


Figure 6b: EPC2106-Q2: Gate Charge

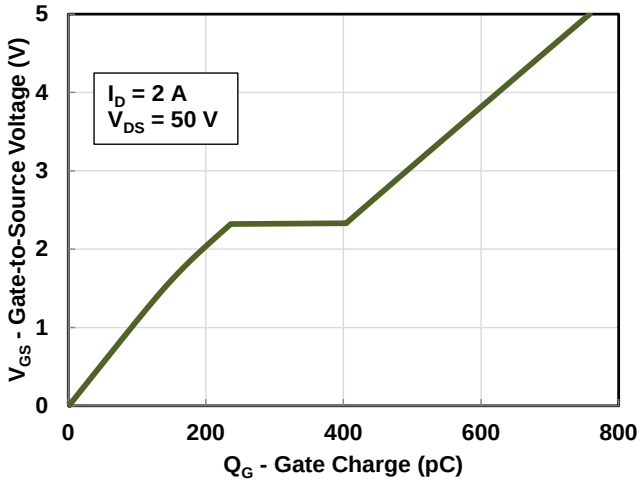


Figure 7a: EPC2106-Q1: Reverse Drain-Source Characteristics

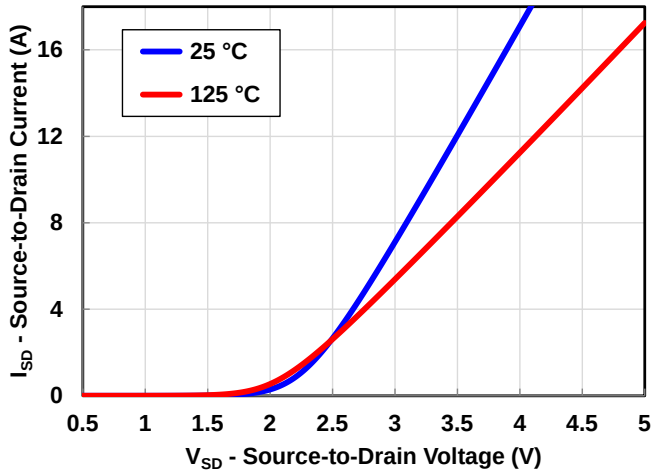


Figure 7b: EPC2106-Q2: Reverse Drain-Source Characteristics

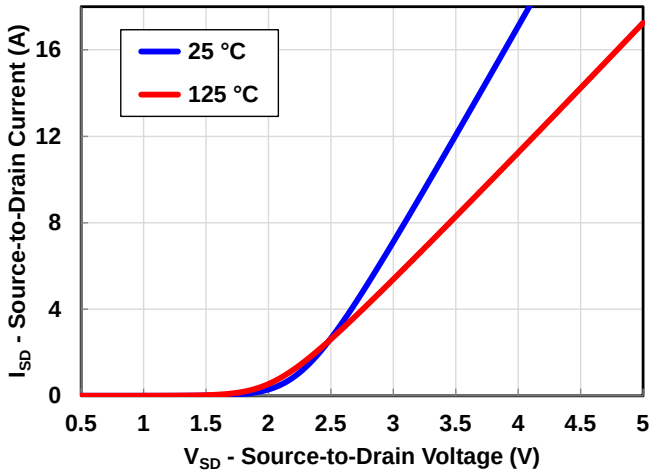


Figure 8a: EPC2106-Q1: Normalized On Resistance vs. Temperature

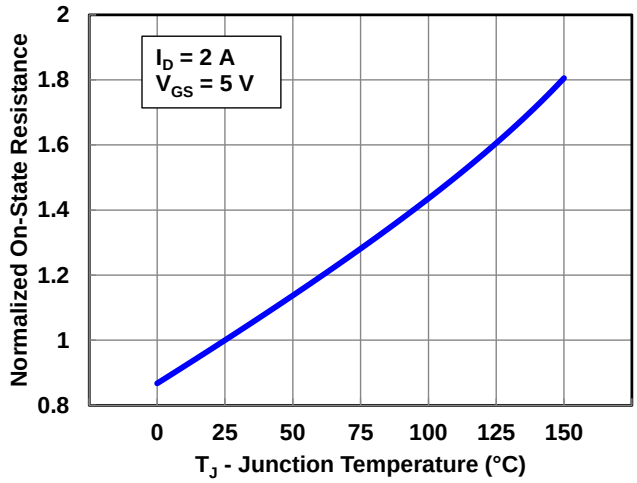


Figure 8b: EPC2106-Q2: Normalized On Resistance vs. Temperature

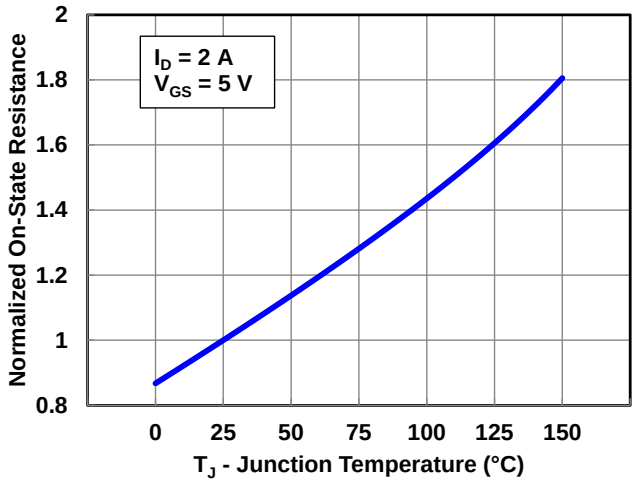


Figure 9a:
EPC2106-Q1: Normalized Threshold Voltage vs. Temperature

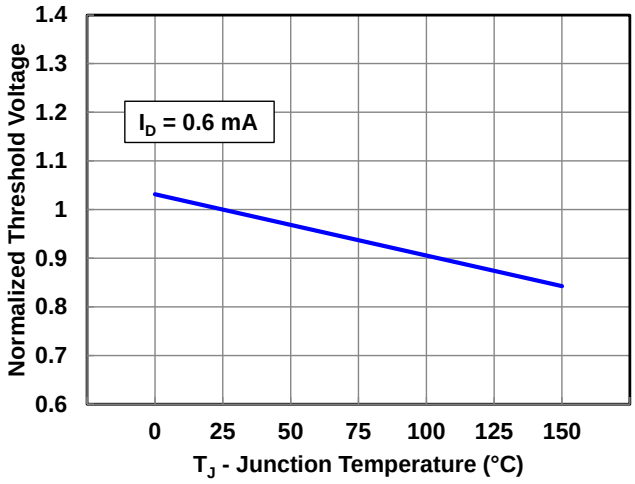
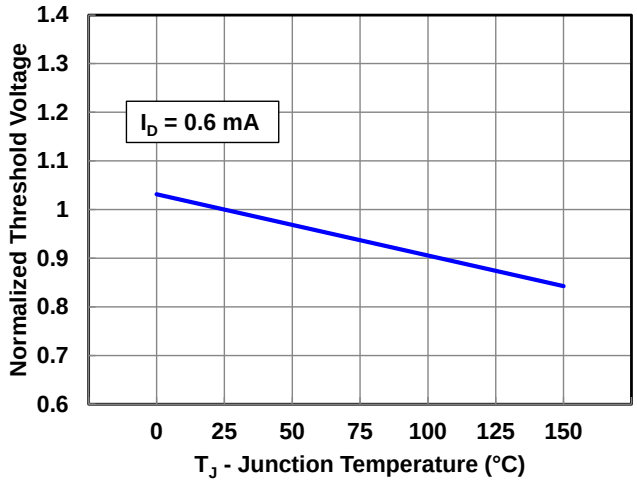
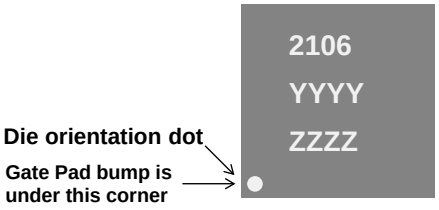


Figure 9b:
EPC2106-Q2: Normalized Threshold Voltage vs. Temperature



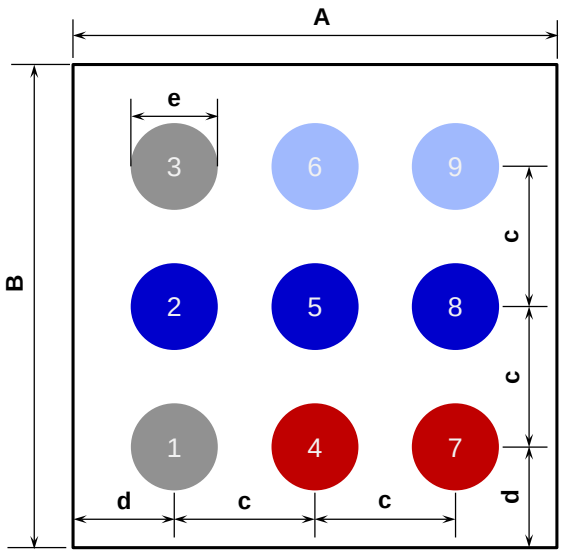
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2106ENGR	2106	YYYY	ZZZZ

DIE OUTLINE

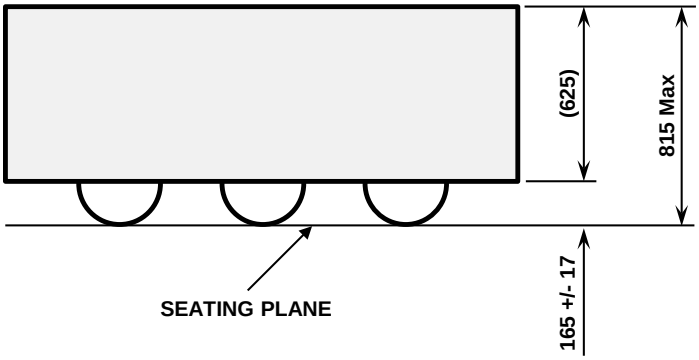
Solder Ball View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

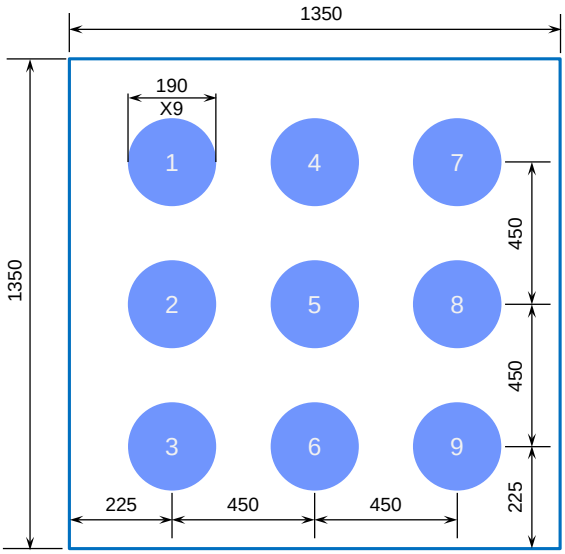
Pad 1 is Gate1 (high side);
Pad 3 is Gate2 (low side);
Pads 4, 7 are V_{IN};
Pads 2, 5, 8 are Switch Node;
Pads 6, 9 are Ground.

Side View



RECOMMENDED LAND PATTERN

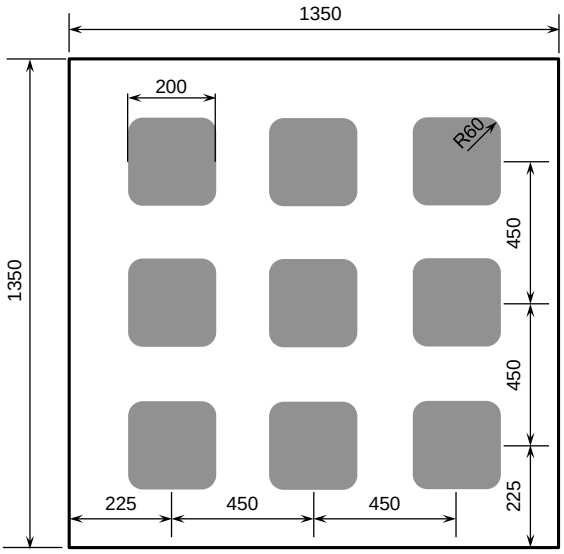
(Units in µm)



Pad 1 is Gate1 (high side);
Pad 3 is Gate2 (low side);
Pads 4, 7 are V_{IN};
Pads 2, 5, 8 are Switch Node;
Pads 6, 9 are Ground.

RECOMMENDED STENCIL DESIGN

(Units in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content
Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised December, 2015