Octal Bus Buffer

The MC74VHC541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC541 is a noninverting type. When either $\overline{OE1}$ or OE2 are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 3.7 \text{ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4 \mu A$ (Max) at $T_A = 25^{\circ}C$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

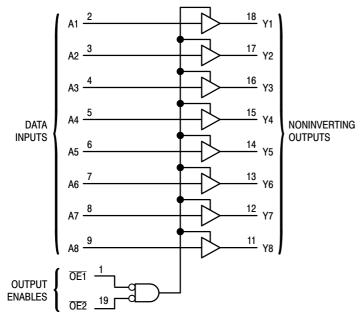
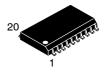


Figure 1. Logic Diagram



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SOIC-20WB **SUFFIX DW** CASE 751D



TSSOP-20 **SUFFIX DT** CASE 948E



SOEIAJ-20 **SUFFIX M CASE 967**

PIN ASSIGNMENT

OE1 [1●	20	v _{cc}
A1 [2	19	OE2
A2 [3	18] Y1
A3 [4	17] Y2
A4 [5	16] Y3
A5 [6	15] Y4
A6 [7	14] Y5
A7 [8	13] Y6
A8 [9	12] Y7
GND [10	11] Y8
			•

FUNCTION TABLE

	Inputs	Output V	
OE1	OE2	Α	Output Y
L L H X	LXH	L H X X	L H Z Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Paramete	Value	Unit	
V _{CC}	DC Supply Voltage		- 0.5 to + 7.0	V
V _{in}	DC Input Voltage		- 0.5 to + 7.0	V
V _{out}	DC Output Voltage		- 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	- 20	mA	
I _{OK}	Output Diode Current	± 20	mA	
l _{out}	DC Output Current, per Pin		± 25	mA
I _{CC}	DC Supply Current, V _{CC} and G	ND Pins	± 50	mA
P _D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature		- 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time V_{CC} = 3.3V ± 0.3 V V_{CC} = 5.0V ± 0.5 V	0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

			V	T _A = 25°C			T _A = - 55	to 125°C	
Symbol	Parameter	Test Conditions	V _{CC}	Min	Тур	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} x 0.7			1.50 V _{CC} x 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} x 0.3		0.50 V _{CC} x 0.3	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$\begin{aligned} V_{in} &= V_{IH} \text{ or } V_{IL} \\ I_{OH} &= -4\text{mA} \\ I_{OH} &= -8\text{mA} \end{aligned}$	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$\begin{aligned} V_{in} &= V_{IH} \text{ or } V_{IL} \\ I_{OL} &= 4mA \\ I_{OL} &= 8mA \end{aligned}$	3.0 4.5			0.36 0.36		0.44 0.44	
l _{in}	Maximum Input Leakage Current	V _{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μΑ
I _{OZ}	Maximum 3–State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5	μΑ
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	μА

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

					Γ _A = 25°(;	T _A = - 55	to 125°C	
Symbol	Parameter	Test Condi	itions	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		5.0 7.5	7.0 10.5	1.0 1.0	8.5 12.0	ns
		$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15pF$ $C_L = 50pF$		3.5 5.0	5.0 7.0	1.0 1.0	6.0 8.0	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Y	$\begin{aligned} V_{CC} &= 3.3 \pm 0.3 V \\ R_L &= 1 k \Omega \end{aligned}$	$C_L = 15pF$ $C_L = 50pF$		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		$\begin{aligned} V_{CC} &= 5.0 \pm 0.5 V \\ R_L &= 1 k \Omega \end{aligned}$	$C_L = 15pF$ $C_L = 50pF$		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Y	$\begin{aligned} V_{CC} &= 3.3 \pm 0.3 V \\ R_L &= 1 k \Omega \end{aligned}$	C _L = 50pF		11.2	15.4	1.0	17.5	ns
		$\begin{aligned} &V_{CC} = 5.0 \pm 0.5 V \\ &R_L = 1 k \Omega \end{aligned}$	C _L = 50pF		6.0	8.8	1.0	10.0	
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 3.3 ± 0.3V (Note 1)	C _L = 50pF			1.5		1.5	ns
		V _{CC} = 5.0 ± 0.5V (Note 1)	C _L = 50pF			1.0		1.0	ns
C _{in}	Maximum Input Capacitance				4	10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)				6				pF
				Typical @ 25°C, V _{CC} = 5.0V					

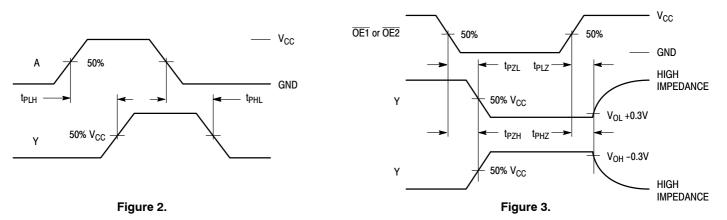
рF

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Power Dissipation Capacitance (Note 2)

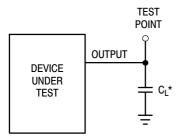
		T _A = 25°C		
Symbol	Parameter	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.9	1.2	٧
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	- 0.9	- 1.2	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

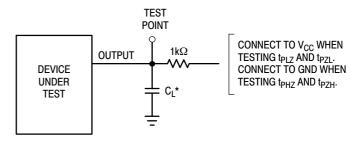


Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
 C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per bit). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

TEST CIRCUITS



*Includes all probe and jig capacitance



*Includes all probe and jig capacitance Figure 5.

Figure 4.

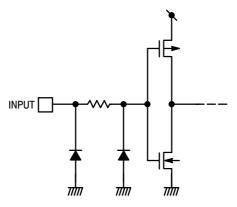


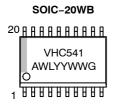
Figure 6. Input Equivalent Circuit

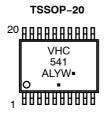
ORDERING INFORMATION

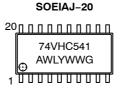
Device	Package	Shipping [†]
MC74VHC541DWR2G	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHC541DTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74VHC541DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC74VHC541MELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS







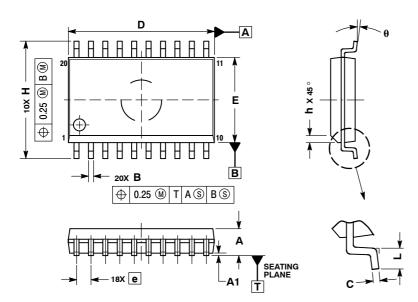
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year

WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

SOIC-20 WB **DW SUFFIX** CASE 751D-05 ISSUE G

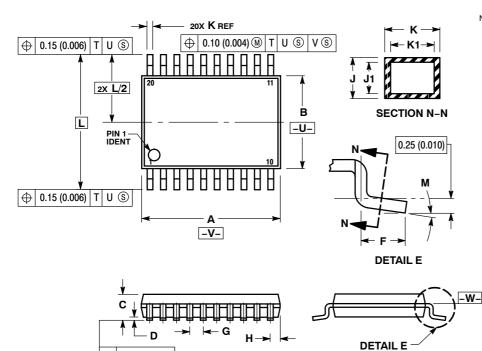


- NOTES:
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION. CONDITION.

	MILLIN	IETERS
DIM	MIN	MAX
Α	2.35	2.65
A1	0.10	0.25
В	0.35	0.49
С	0.23	0.32
D	12.65	12.95
E	7.40	7.60
е	1.27	BSC
Н	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7 °

PACKAGE DIMENSIONS

TSSOP-20 CASE 948E-02 **ISSUE C**



<u>0.100 (0.004)</u>

-T- SEATING PLANE

- NOTES:

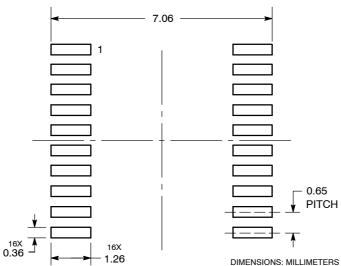
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION:
 MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE
 MOLD FLASH, PROTRUSIONS OR GATE
 BURRS. MOLD FLASH OR GATE BURRS
 SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE
 - SHALL NOT EXCEED 1.13 (J.J.004) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION
 SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 - DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
 - CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

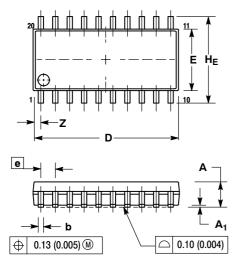
	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

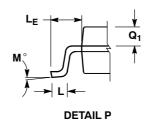
SOLDERING FOOTPRINT

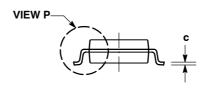


PACKAGE DIMENSIONS

SOEIAJ-20 **M SUFFIX CASE 967 ISSUE A**







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y 14.3M, 1962.

 CONTROLLING DIMENSION: MILLIMETER.

 DIMENSIONS D AND E DO NOT INCLUDE

 MOLD FLASH OR PROTRUSIONS AND ARE

 MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- i. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10°
Q_1	0.70	0.90	0.028	0.035
Z		0.81		0.032

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