

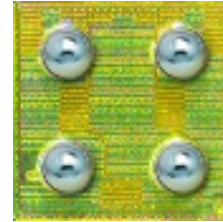
EPC2037 – Enhancement Mode Power Transistor

Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS} , 100V
- Maximum $R_{DS(on)}$, 550 m Ω
- I_D , 1 A
- Pb-Free (RoHS Compliant), Halogen Free



Applications:

- High Frequency DC-DC Conversion
- Wireless Power Transfer
- LiDAR/Pulsed Power Applications
- Class-D Audio

EPC2037 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 0.9 mm x 0.9 mm

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	100 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, ($T_A = 25\text{ }^\circ\text{C}$, $R_{\theta JA} = 120\text{ }^\circ\text{C/W}$)	1 A
Maximum Pulsed Drain Current, 25 °C, $T_{pulse} = 300\text{ }\mu\text{s}$	2.4 A
Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	0.1 mA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.1\text{ A}$	550 m Ω
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.1\text{ A}$	400 m Ω
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.08\text{ mA}$	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	1 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-0.1 mA

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated
 Specifications are with Substrate shorted to Source

EPC2037 – Enhancement Mode Power Transistor Preliminary Specification Sheet



DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	12.5 pF
C_{OSS} (Output Capacitance)		6 pF
C_{RSS} (Reverse Transfer Capacitance)		0.1 pF
Q_G (Total Gate Charge)	$V_{DS} = 50\text{ V}, I_D = 0.1\text{ A}, V_{GS} = 5\text{ V}$	115 pC
Q_{GS} (Gate to Source Charge)	$V_{DS} = 50\text{ V}, I_D = 0.1\text{ A}$	30 pC
Q_{GD} (Gate to Drain Charge)		23 pC
$Q_{G(TH)}$ (Gate Charge at Threshold)		27 pC
Q_{OSS} (Output Charge)	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	530 pC
Q_{RR} (Source-Drain Recovery Charge)		0

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated

Specifications are with Substrate shorted to Source

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	14	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	79	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	$^\circ\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

EPC2037 – Enhancement Mode Power Transistor

Preliminary Specification Sheet



Figure 1: Typical Output Characteristics at 25°C

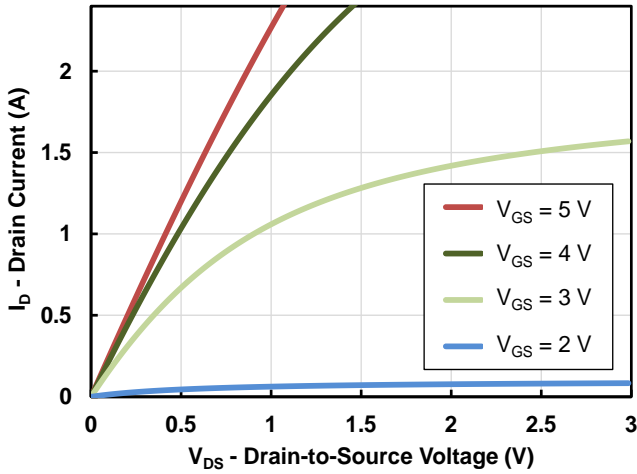


Figure 2: Transfer Characteristics

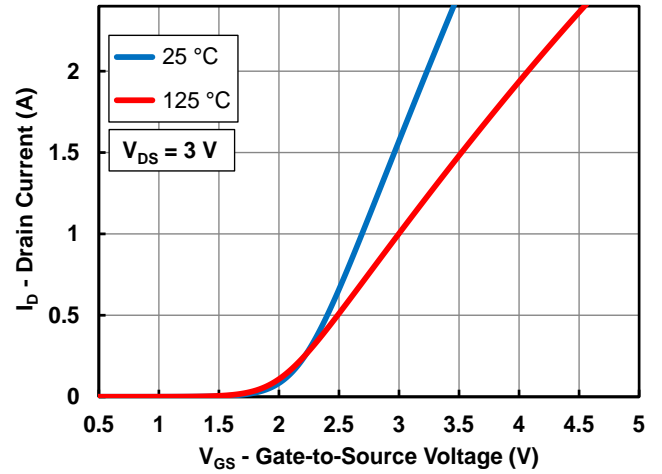


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

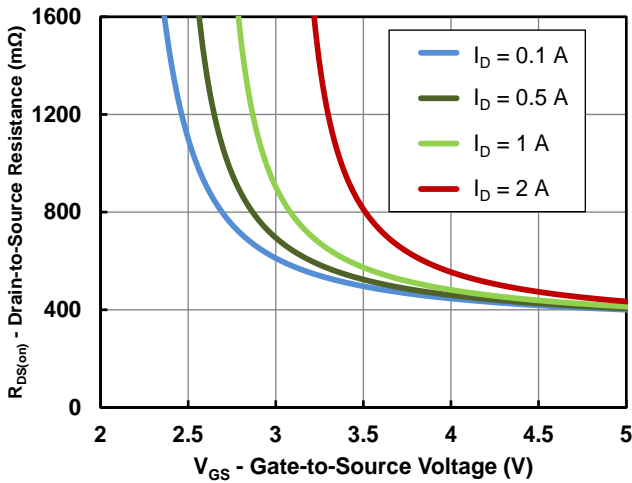


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

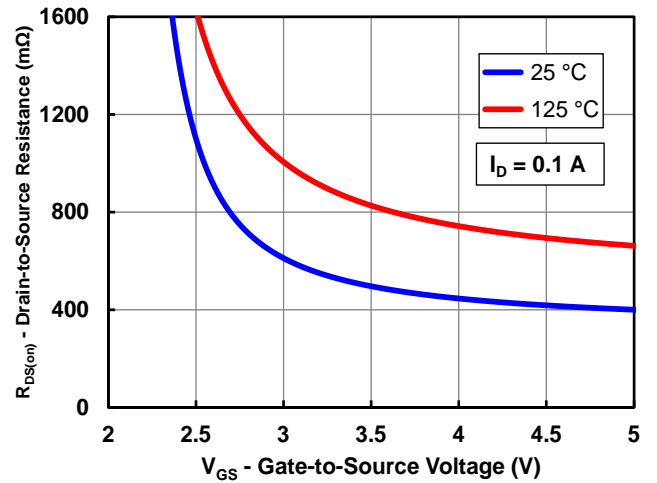


Figure 5a: Capacitance (Linear Scale)

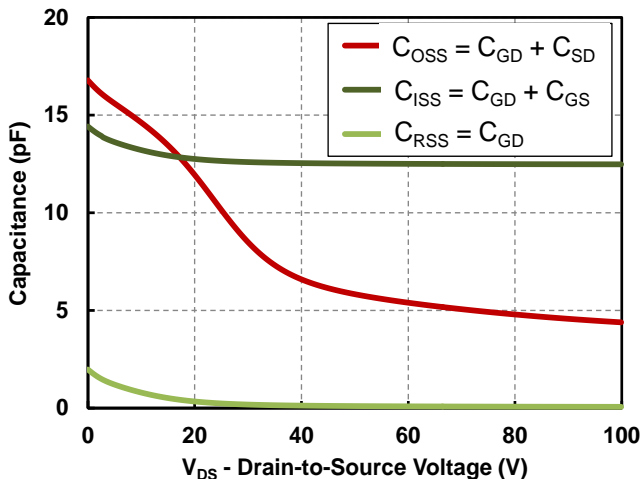
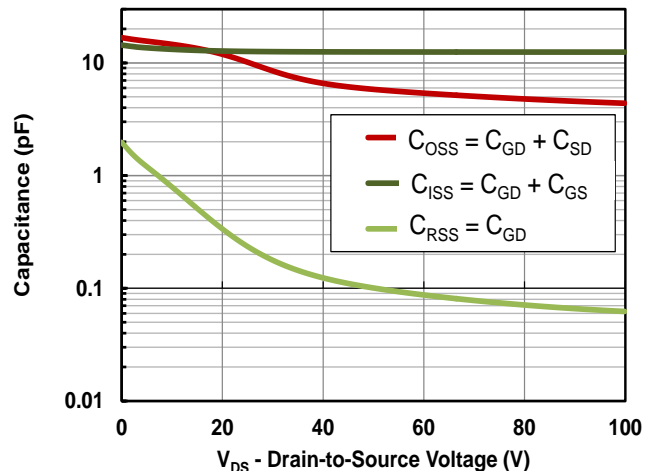


Figure 5b: Capacitance (Log Scale)



EPC2037 – Enhancement Mode Power Transistor

Preliminary Specification Sheet



Figure 6: Gate Charge

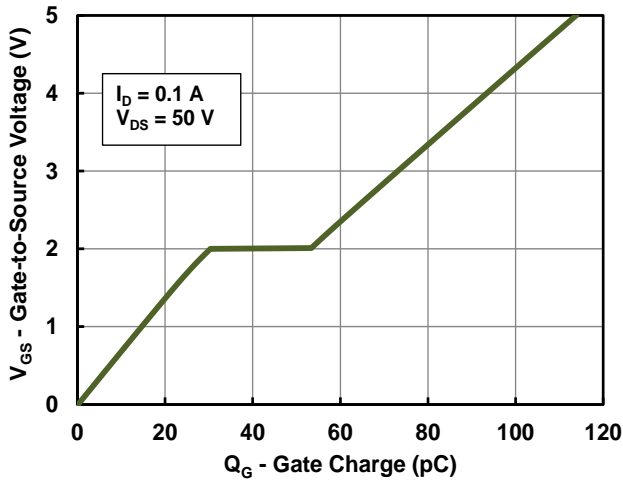


Figure 7: Reverse Drain-Source Characteristics

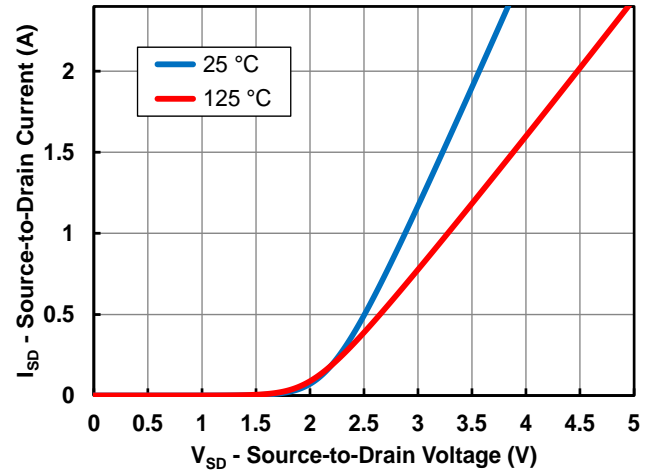


Figure 8: Normalized On Resistance vs. Temperature

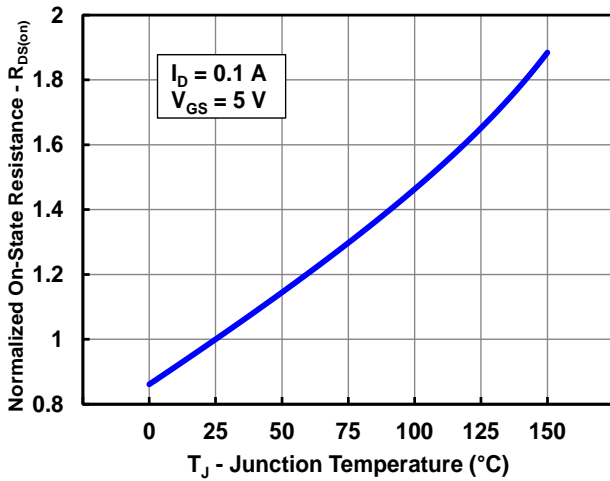


Figure 9: Normalized Threshold Voltage vs. Temperature

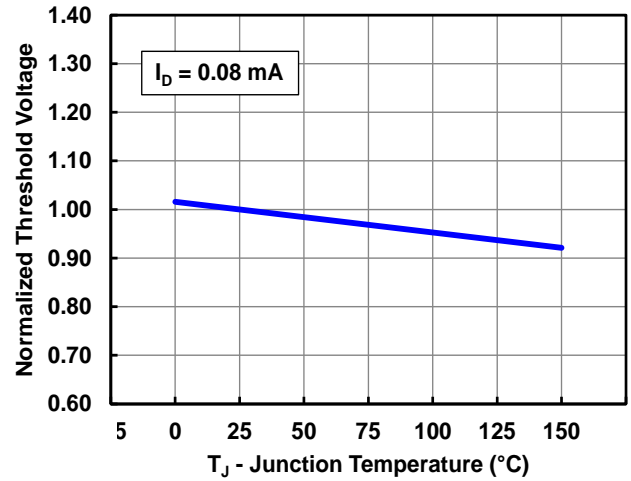
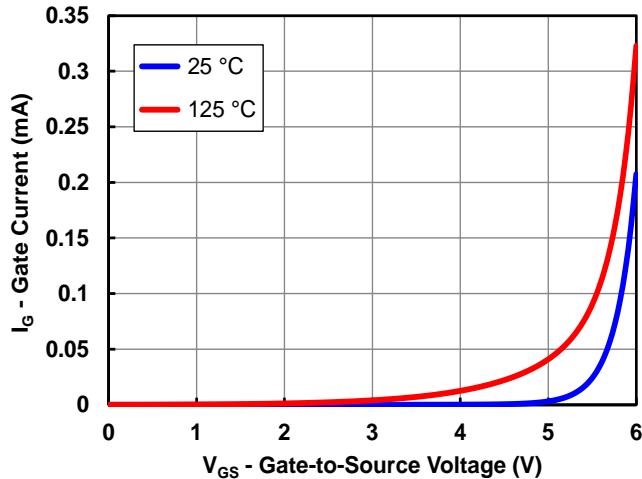


Figure 10: Gate Current

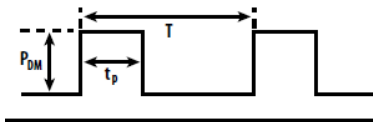
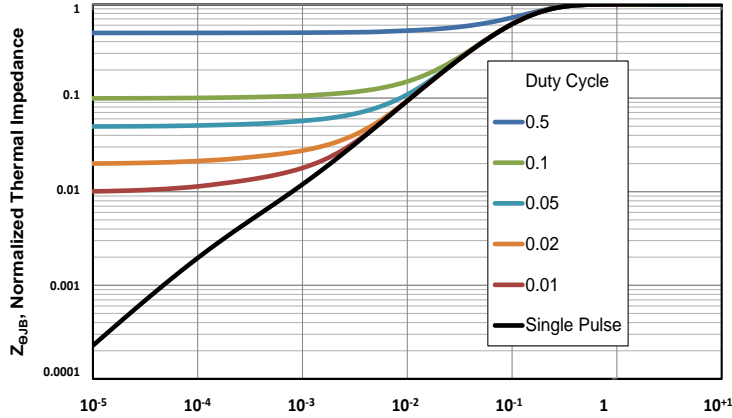


All measurements were done with substrate shorted to source

EPC2037 – Enhancement Mode Power Transistor Preliminary Specification Sheet

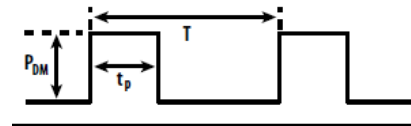
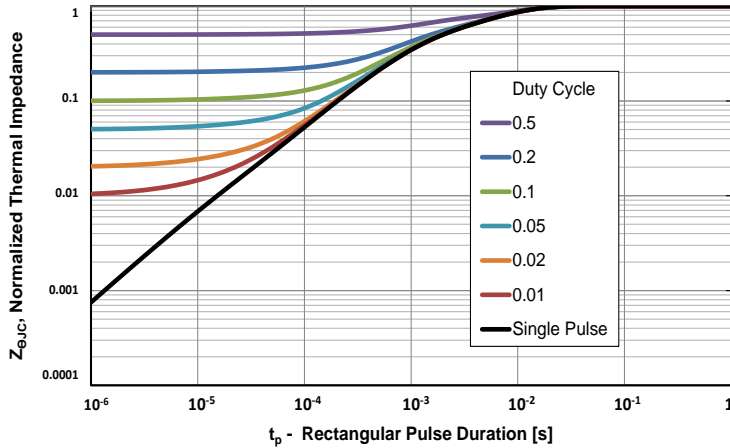
Figure 11: Transient Thermal Response Curves

Junction-to-Board



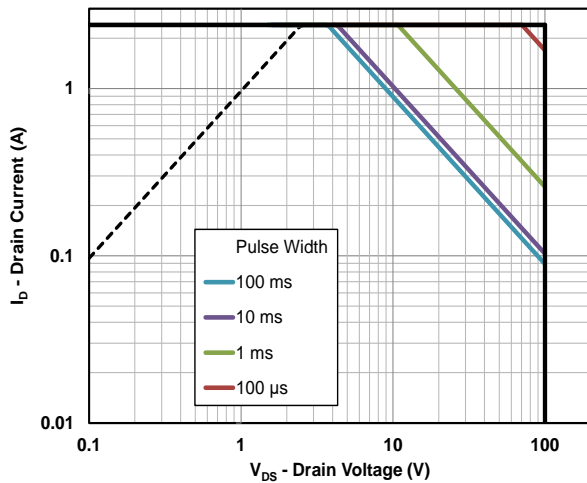
Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Junction-to-Case



Notes:
Duty Factor = t_p/T
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 12: Safe Operating Area



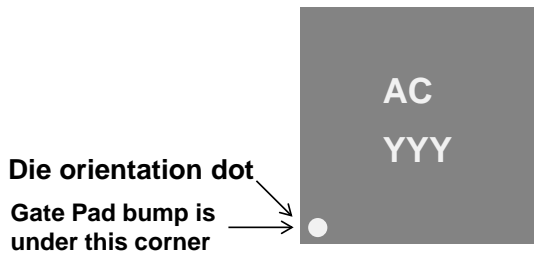
$T_J = \text{Max Rated}, T_C = +25^\circ\text{C}, \text{Single Pulse}$

EPC2037 – Enhancement Mode Power Transistor

Preliminary Specification Sheet



DIE MARKINGS

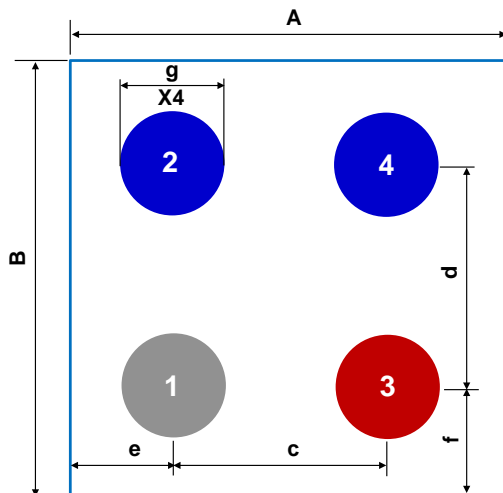


Part Number	Laser Marking	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2037ENGR	AC	YYY

DIE OUTLINE

Solder Bar View

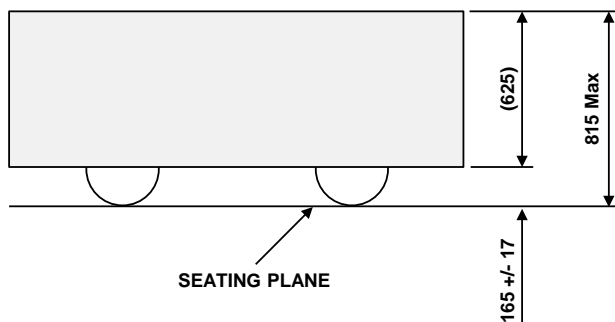
All measurements in micrometers (μm)



Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View

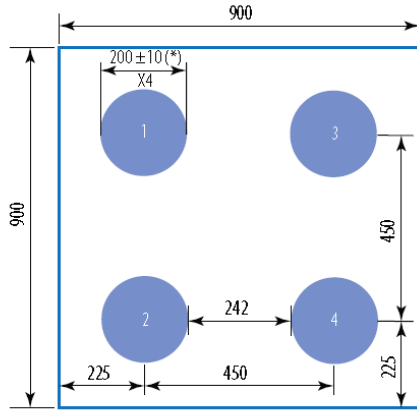


EPC2037 – Enhancement Mode Power Transistor

Preliminary Specification Sheet

RECOMMENDED LAND PATTERN

(Units in μm)



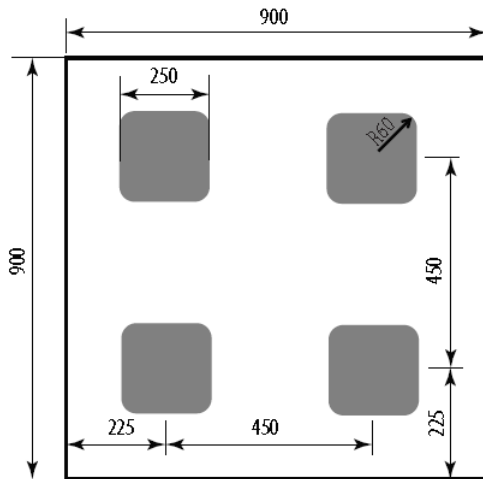
* minimum 190

The land pattern is solder mask defined
Solder mask is 10 μm smaller per side than bump

Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

RECOMMENDED STENCIL

(Units in μm)



Recommended stencil should be 4mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein. Engineering devices, designated with an ENG* suffix at point of purchase, are first article products that EPC is preparing for production release. Specifications may change on final production release of the device. If you have questions please [contact us](#). EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of other.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.

U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

Revised February, 2017