74LVTH322245

3.3 V 32-bit bus transceiver with 30 Ω termination resistors; 3-state

Rev. 01 — 24 January 2007 Product data sheet

1. General description

The 74LVTH322245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. The 74LVTH322245 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters. The 74LVTH322245 is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ($n\overline{OE}$) inputs for easy cascading and four send/receive (nDIR) inputs for direction control. Pin $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features

- 32-bit bidirectional bus interface
- 3-state buffers
- Output capability: +12 mA and −12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Outputs include series resistance of 30 Ω making external resistors unnecessary
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78 Class II level A exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVTH322245EC	−40 °C to +125 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

NXP founded by Philips

4. Functional diagram

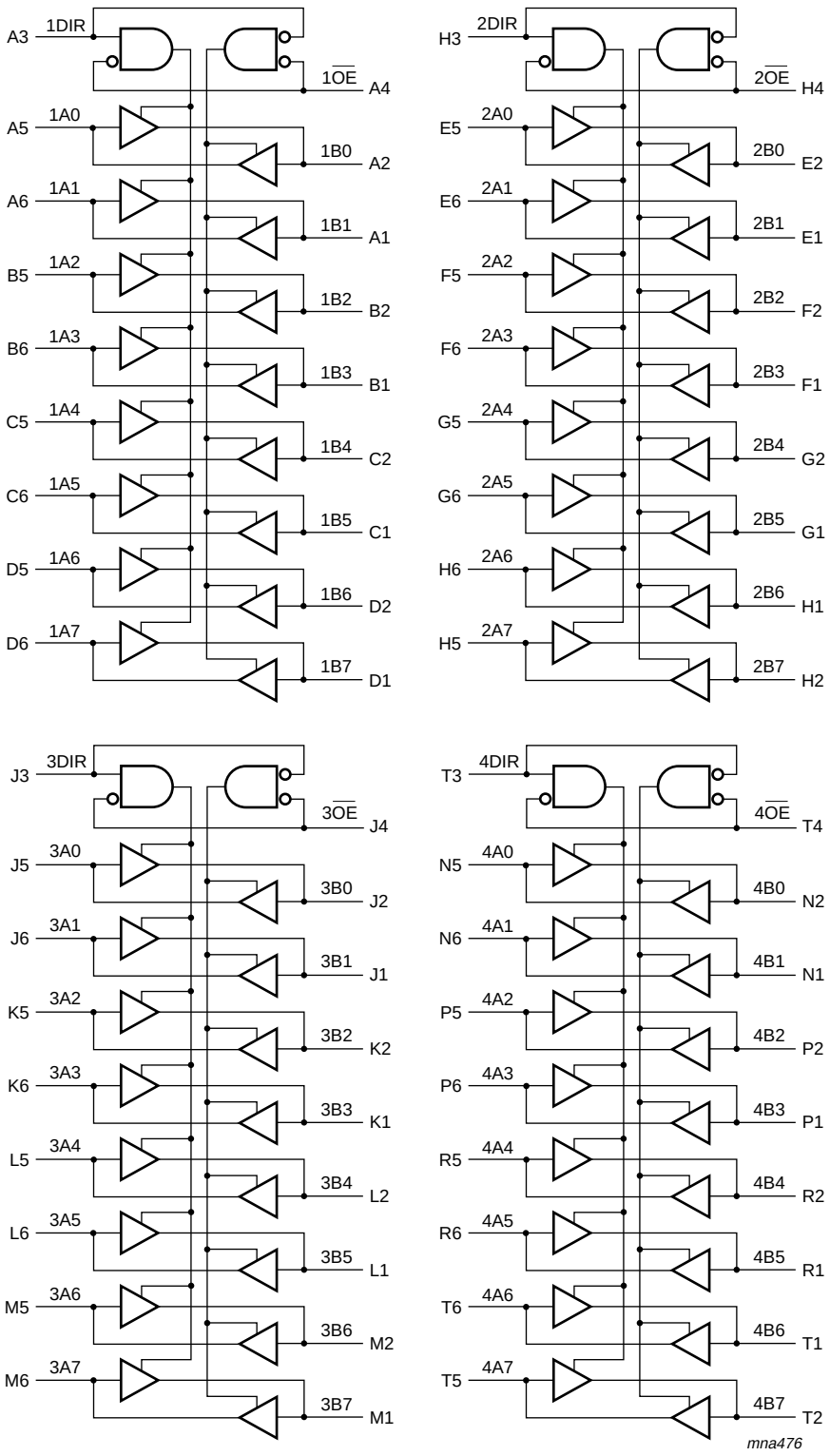

Fig 1. Logic symbol

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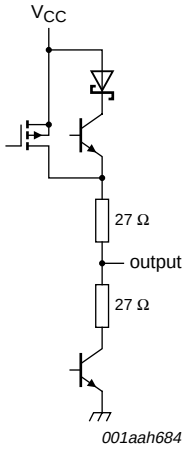

Fig 2. Schematic of each output

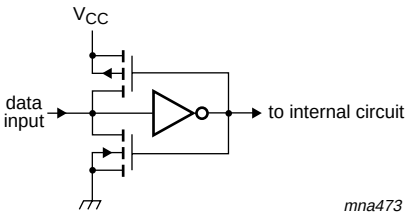

Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning

mna475

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A6	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A6
5	1A0	1A2	1A4	1A6	2A0	2A2	2A4	2A7	3A0	3A2	3A4	3A6	4A0	4A2	4A4	4A7
4	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
3	1DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	2DIR	3DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	4DIR
2	1B0	1B2	1B4	1B6	2B0	2B2	2B4	2B7	3B0	3B2	3B4	3B6	4B0	4B2	4B4	4B7
1	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B6	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B6

Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
$n\overline{OE}$ (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output

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Table 2. Pin description *...continued*

Symbol	Ball	Description
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V_{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

6. Functional description

Table 3. Function selection[1]

Input		Input/output	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[3]	–0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH-state	[3]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		–64	-	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond indicated under Section 8 "Recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.7	-	3.6	V
V_I	input voltage			0	-	5.5	V
I_{OH}	HIGH-level output current			–12	-	-	mA
I_{OL}	LOW-level output current			-	-	12	mA
T_{amb}	ambient temperature	in free air		–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled		-	-	10	ns/V
P_{tot}	total power dissipation		[1]	-	-	1000	mW

[1] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C	[1]						
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		–1.2	–0.85	-	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = –12 mA		2.0	2.5	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 12 mA		-	0.3	0.8	V
I_I	input leakage current	control pins					
		V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.1	10	µA
		input/output data pins; V_{CC} = 3.6 V	[2]				
		V_I = V_{CC}		-	0.5	10	µA
		V_I = 0 V		–5	–0.1	-	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA
I_{LO}	output leakage current	output HIGH; V_O = 5.5 V; V_{CC} = 3.0 V		-	75	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-	40	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V		75	135	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V		-	–135	–75	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	[3]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	[3]	-	-	–500	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.14	0.24	mA
		outputs LOW		-	8.4	12	mA
		outputs disabled	[5]	-	0.14	0.24	mA

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_I	input capacitance	control pins; V_O = 0 V or 3.0 V		-	3	-	pF
$C_{I/O}$	input/output capacitance	input/output data pins; outputs disabled; V_{CC} = 3.6 V; I_O = 0 A; V_I = GND or V_{CC}		-	9	-	pF

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C unless otherwise specified.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus-hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for load circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PLH}	LOW to HIGH propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		V_{CC} = 2.7 V	-	-	3.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		V_{CC} = 2.7 V	-	-	3.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.2	3.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nAn or nBn; see Figure 6				
		V_{CC} = 2.7 V	-	-	6.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.5	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nAn or nBn; see Figure 6				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	4.4	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Figure 6				
		V_{CC} = 2.7 V	-	-	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.5	4.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Figure 6				
		V_{CC} = 2.7 V	-	-	5.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	4.3	6.7	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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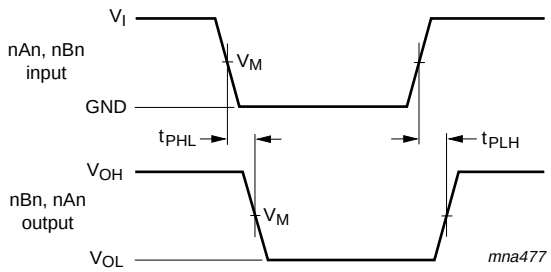
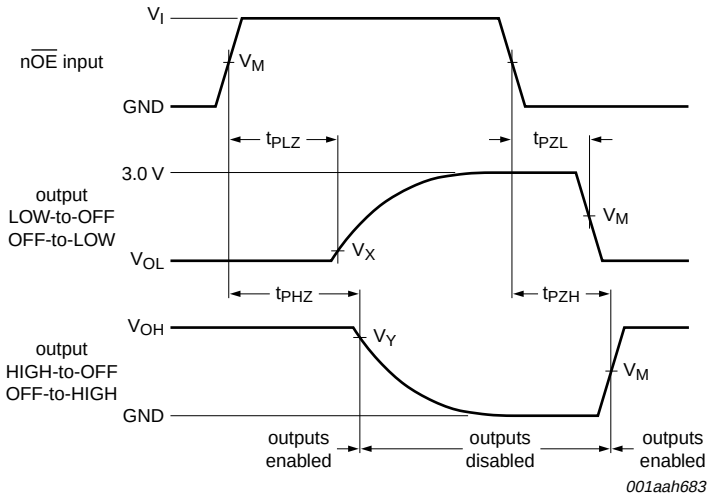
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.7 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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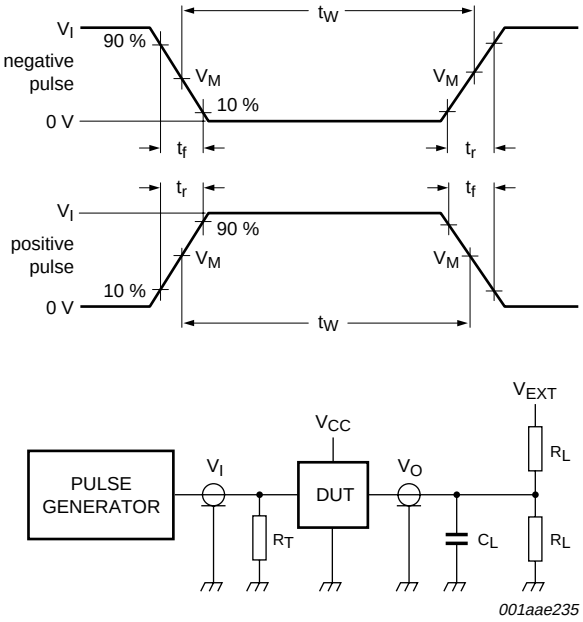

Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Load circuitry for switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

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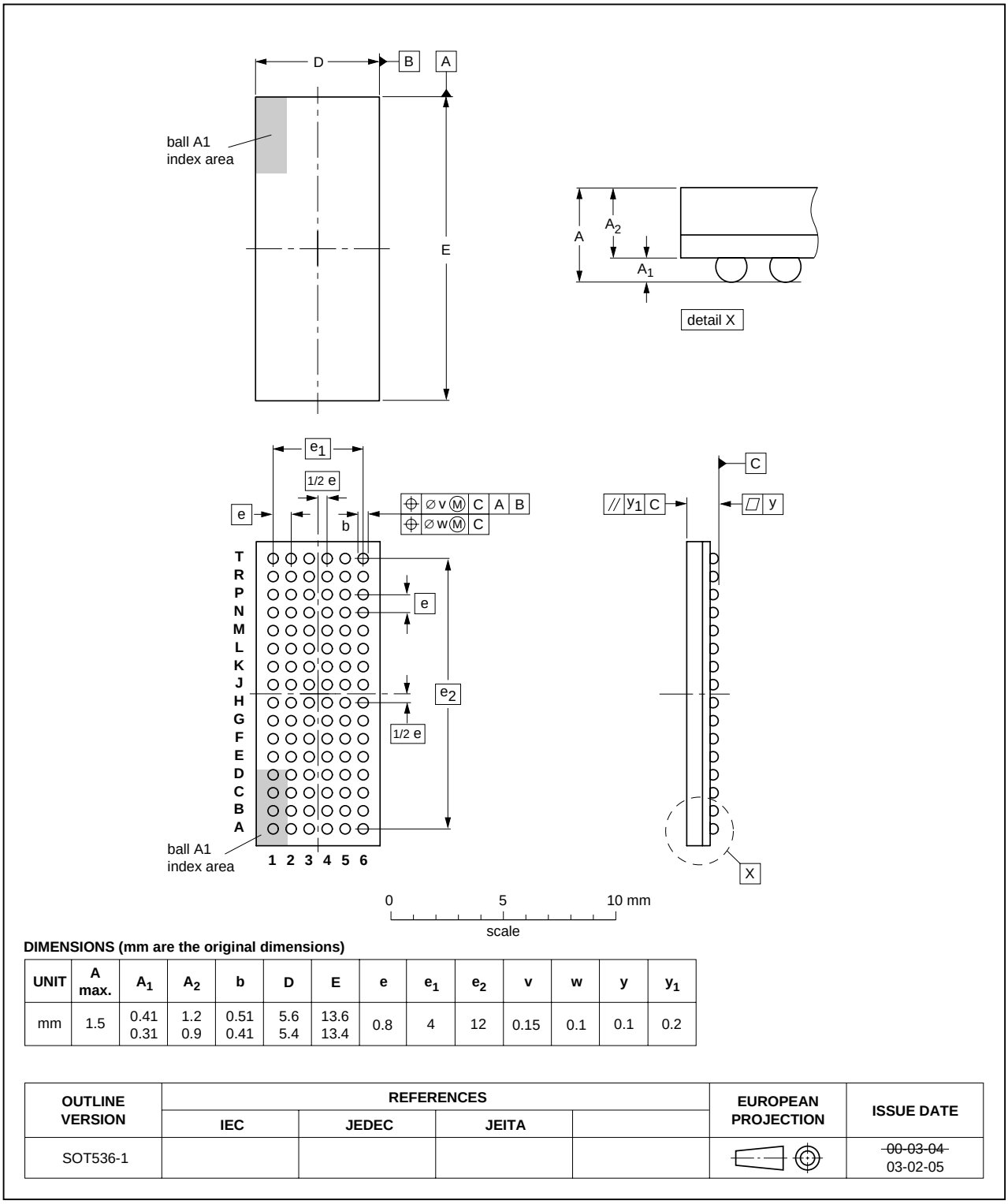
12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 8. Package outline SOT536-1 (LFBGA96)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVTH322245_1	20080124	Product data sheet	-	-

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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