CEL California Eastern Laboratories

Evaluation Board Document

NE5550779A-EV04-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- o Circuit Schematic and Assembly Drawing

Circuit Description

The NE5550779A-EV04-A is an evaluation circuit board for Renesas' LDMOS power FET, NE5550779A optimized for the performance at 460MHz. The circuit board is RoHS compliant.

Matching and Bias Circuits

Both input and output matching networks consist of shunt capacitors and sections of transmission lines (refer to the schematic and assembly drawing in the two last pages for the component designation). The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve optimal performance. For applications where there is a constraint on the board space, a serial inductor, instead of transmission lines, can be used for the matching circuits. The efficiency spec, PAE, usually will be slightly lower in that case.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of $k\Omega$, can be used for the bias at gate so that the RF path is completely isolated from the DC line. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 140mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

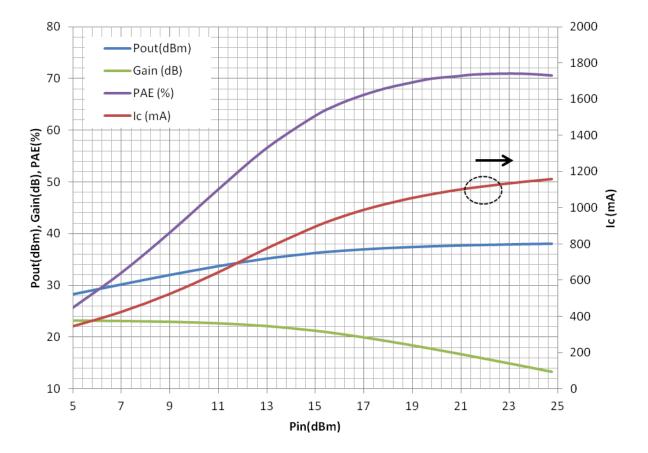
Typical Performance Data

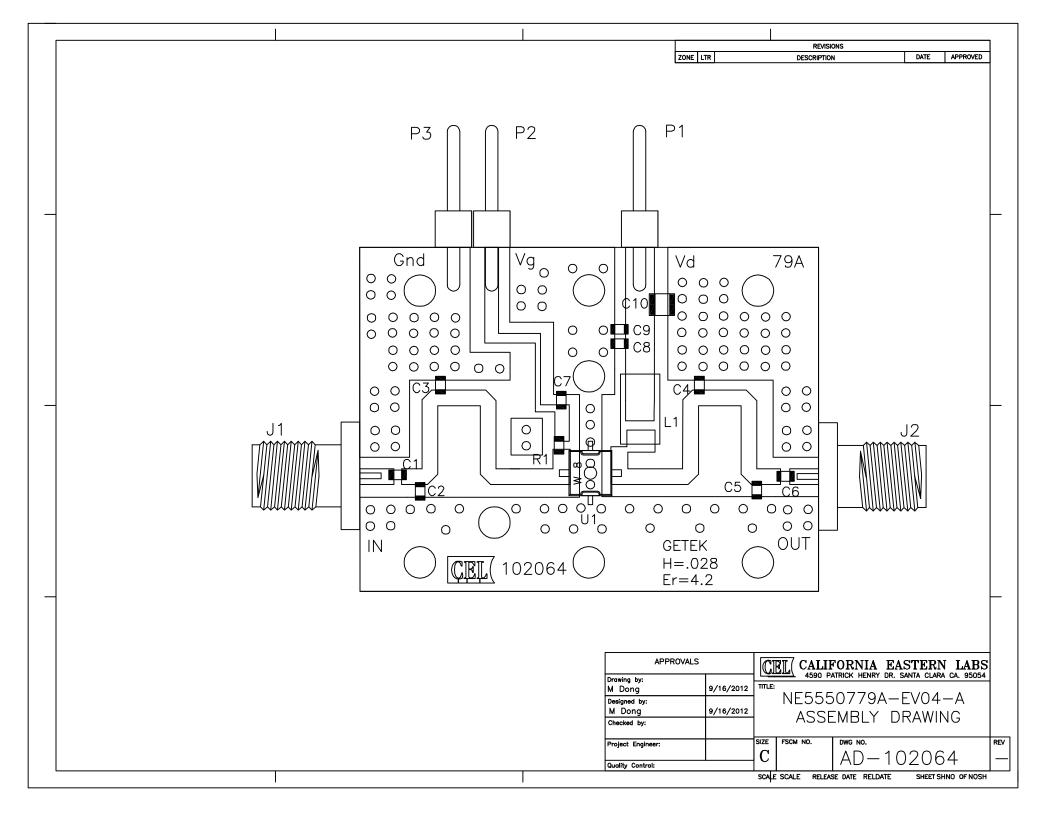
Test Conditions:

f=460MHz

Vd=7.5V, Idsq=140mA

Pout, Gain, PAE and Current vs Pin are shown in the following plot.





						1		PEVIS	SIONS		
						ZONE LTR		DESCRIPTI		DATE	APPROVED
	RF		$\begin{array}{c} V_{g} & V_{d} \\ & & \\ &$	- C ¹	9 8 <u>C4</u> <u>TL4</u> <u><u><u></u></u>10.5</u>	 C5	C6 	RF out -O			
	Note: A	6.8pF I transmission line secti	22pF U1 NE5550779A ons are 50ohm and their electrical lengths ar	e at 4	15рҒ 460мнz	0.601	Γ				
	Note: A		22pF U1 NE5550779A	e at 4		0.601	Γ				
1	Note: A TF-101964		22pF U1 NE5550779A	14		0.601	Γ				
1			22pF U1 NE5550779A ons are 50ohm and their electrical lengths ar	14 13		0.641	Γ				
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