CEL California Eastern Laboratories

Evaluation Board Document

NE5550779A-EV04-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- Circuit Schematic and Assembly Drawing

Circuit Description

The NE5550779A-EV04-A is an evaluation circuit board for Renesas' LDMOS power FET, NE5550779A optimized for the performance at 460MHz. The circuit board is RoHS compliant.

Matching and Bias Circuits

Both input and output matching networks consist of shunt capacitors and sections of transmission lines (refer to the schematic and assembly drawing in the two last pages for the component designation). The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve optimal performance. For applications where there is a constraint on the board space, a serial inductor, instead of transmission lines, can be used for the matching circuits. The efficiency spec, PAE, usually will be slightly lower in that case.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of kΩ, can be used for the bias at gate so that the RF path is completely isolated from the DC line. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 140mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

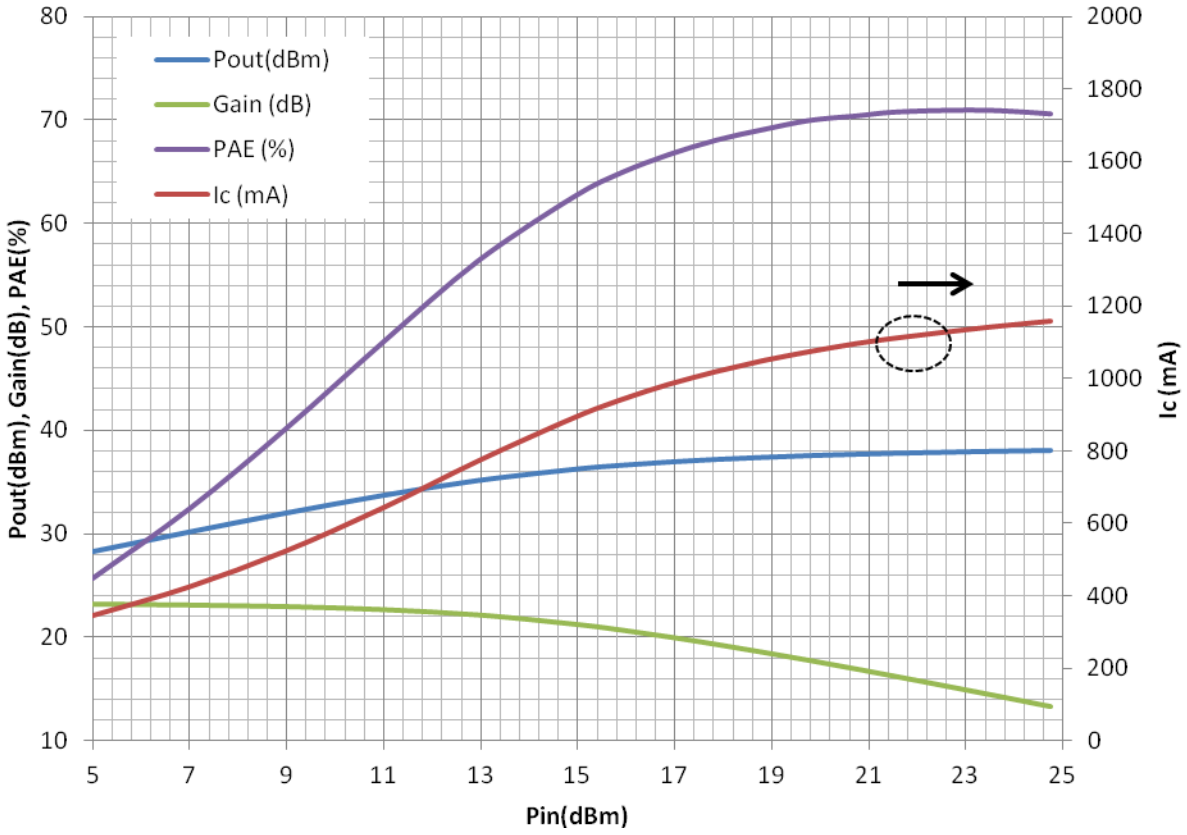
Typical Performance Data

Test Conditions:

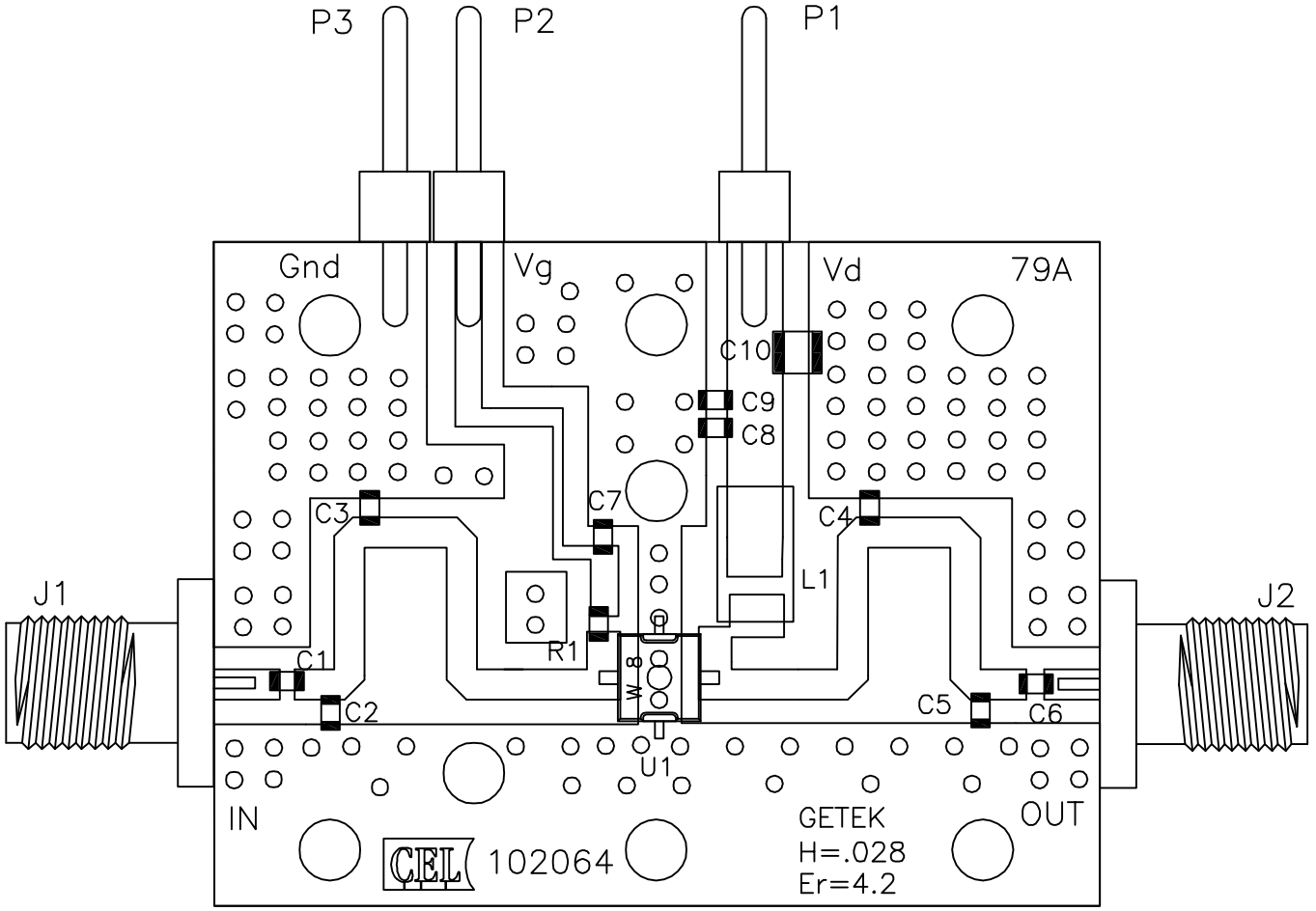
f=460MHz

Vd=7.5V, Idsq=140mA

Pout, Gain, PAE and Current vs Pin are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



APPROVALS		
Drawing by: M Dong	9/16/2012	
Designed by: M Dong	9/16/2012	
Checked by:		
Project Engineer:		
Quality Control:		

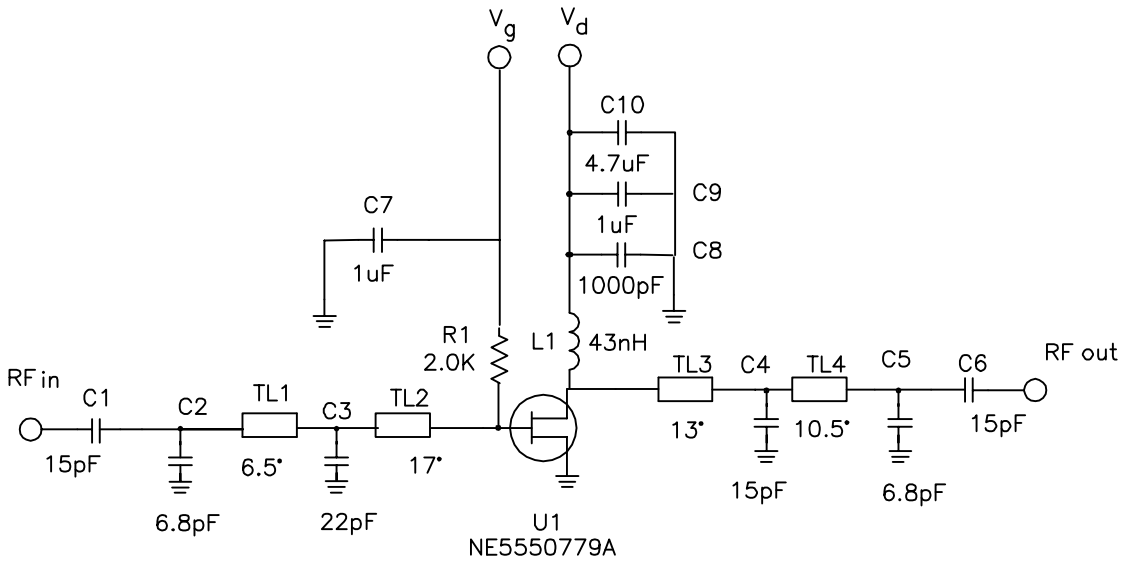
CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
NE5550779A-EV04-A
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-102064	—

SCALE SCALE RELEASE DATE RELDATE SHEET SHNO OF NOSH

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



Note: All transmission line sections are 50ohm and their electrical lengths are at 460MHz

ITEM NO.	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	QTY
14	TF-101964		ALUMINUM BLOCK	1
13	267M1002475K	C10	4.7uF 10V TANT CHIP CAP B MATS	1
12	GRM1885C1H102JA01B+A01	C8	0603 1000pF CAP MURATA	1
11	GRM185R61C105KE44D	C7,C9	0603 1uF CAP MURATA	2
10	GRM1885C1H150JA01B+A01	C4	0603 15pF CAP MURATA	1
9	GRM1885C1H220JA01B+A01	C3	0603 22pF CAP MURATA	1
8	GRM1885C1H6R8DZ01B+C01	C2,C5	0603 6.8pF CAP MURATA	2
7	GRM1885C1H150JA01B+A01	C1,C6	0603 15pF CAP MURATA	2
6	GENERIC	R1	0603 2.0KOHM RESISTOR	1
5	B10TJ	L1	43nH INDUCTOR COILCRAFT	1
4	2340-6111 TG	P1,P2,P3	PIN HEADER 3M	3
3	5308-2CC	J1,J2	SMA 4H FLANGE JACK TENSOLITE	2
2	NE5550779A-A	U1	RENESAS NE5550779A-A	1
1	CL-102064	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

APPROVALS		
Drawing by: MDONG	9/16/2012	
Designed by: MDONG	9/16/2012	
Checked by:		
Project Engineer:		
Quality Control:		

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TITLE:
NE5550779A-EV04-A
SCHEMATIC AND BOM

SIZE	FSCM NO.	DWG NO.	REV
C		AD-102064	

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