

Disc	continued Product
These parts are no los purchased for new de	nger in production The device should not be esign applications. Samples are no longer available.
Date of status change	e: December 1, 2015
Recommended S	ubstitutions:
For existing custome cations, refer to the <u>A</u>	<i>r transition, and for new customers or new appli- <u>ITS128</u>.</i>
NOTE: For detailed i local Allegro field ap	information on purchasing options, contact your oplications engineer or sales representative.

Allegro MicroSystems, LLC reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Features and Benefits

- Chopper Stabilization
- Extremely low switchpoint drift over temperature
- On-chip Protection
- Supply transient protection
- Output short-circuit protection
- Reverse-battery protection
- True Zero-Speed Operation
- True Power-On State
- Single-chip Sensing IC for High Reliability
- Optimized Magnetic Circuit
- Wide Operating Voltage Range
- Internal Regulator

Package: 4-pin SIP (suffix SE)



Not to scale

Description

The ATS636LSE programmable, true power-on state (TPOS), device is optimized Hall-effect IC and rare-earth pellet combinations that switch in response to magnetic signals created by ferromagnetic targets in gear-tooth sensing and proximity applications.

The device is externally programmable. A wide range of programmability is available on the magnetic operate point (B_{OP}) while the hysteresis remains fixed. This advanced feature allows for optimization of the circuit switchpoint and can drastically reduce the effects of mechanical placement tolerances found in production environments .

A proprietary dynamic offset cancellation technique, with an internal high-frequency clock, reduces the residual offset voltage, which is normally caused by device overmolding, temperature dependencies, and thermal stress. Having the Hall element and amplifier in a single chip minimizes many problems normally associated with low-level analog signals.

This device is ideal for use in gathering speed or position information using gear-tooth-based configurations, or for proximity sensing with ferromagnetic targets.

Continued on the next page



Functional Block Diagram

Description (continued)

The ATS636LSE has the opposite polarity and switches low in the presence of a ferromagnetic target or tooth and switches high in the presence of a target valley, window, or when the ferromagnetic target is removed.

These devices are lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Output (Tooth)	Packing*			
ATS636LSETN-T	Low	13-in. reel, 450 pieces/reel			
*Contact Allegro [™] for additional packing options.					



Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V _{cc}	Fault conditions that produce supply voltage transients will be clamped by an internal Zener diode. These conditions can be tolerated but should be avoided.		V
Reverse Supply Voltage	V _{RCC}		-18	V
Overvoltage Supply Current	I _{CC}		100	mA
Output Off Voltage	V _{OUT}		26.5	V
Output Sink Current	I _{OUT}	T Internal current limiting is intended to protect the device from output short circuits, but is not intended for continuous operation.		mA
Magnetic Flux Density	В		Unlimited –	
Package Power Dissipation	PD		See Graph	-
Operating Ambient Temperature	T _A	Range L	-40 to 150	°C
Junction Temperature	TJ		165	°C
Storage Temperature Range	T _{stg}		–65 to 170	°C

Pin-out Diagram

Terminal List

Number	Name	Function		
1	VCC	Device supply		
2	VOUT	Device output		
3	NC	No connect		
4	GND	Device ground		





Programmable Back Biased Hall-Effect Switch with TPOS Functionality

ELECTRICAL CHARACTERISTICS over operating voltage and junction temperature range; unless otherwise noted

Characteristics	Symbol	Test Conditions		Typ. ¹	Max.	Unit
Supply Voltage ²	V _{CC}	Operating	4.2	_	24	V
Power-Up State	POS	After programming V _{CC} = 0 × V _{CC} (min), t > t _{ON} : B < B _{OP}	High	High	High	-
Low Output Voltage	V _{OUT(SAT)}	Output on, I _{OUT} = 20 mA	_	175	400	mV
Output Current Limit ³	I _{OUTM}	Pulse test method, output on	30	50	90	mA
Output Leakage Current	I _{OFF}	Output off, V _{OUT} = 24 V	_	_	10	μA
Supply Current	1	Output off (high)	_	2.5	5.5	mA
Supply Current I _{CC}	'CC	Output on (low)	_	2.5	5.5	mA
Reverse Supply Current	I _{RCC}	V _{RCC} = -18 V	-	-	-5	mA
Power-On Delay ⁴	t _{ON}	Output off, $V_{CC} > V_{CC}(min)$		35	50	μs
Output Rise Time	t _r	R _L = 820 Ω, C _L = 10 pF	-	1.2	5	μs
Output Fall Time	t _f	R _L = 820 Ω, C _L = 10 pF	-	1.2	5	μs
Sampling Frequency	f _{sample}		_	250	_	kHz
Supply Zener Voltage	V _{Zsupply}	$I_{CC} = I_{CC}(max) + 3 \text{ mA}, T_A = 25^{\circ}C$	28	_	—	V
Output Zener Voltage	V _{Zoutput}	$I_{OUT} = 3 \text{ mA}, T_A = 25^{\circ}\text{C}$	30	_	_	V
Supply Zener Current ⁵	I _{Zsupply}	V _S = 28 V	_	-	8.5	mA
Output Zener Current	I _{Zoutput}	V _O = 30 V	-	-	3	mA

¹Typical data is at V_{CC} = 12 V and T_A = 25°C. ²Do not exceed the maximum thermal junction temperature: see power derating curve.

³Short circuit protection is not intended for continuous operation and is tested using pulses.

⁴The Power-On Delay is the time that is necessary before the output signal is valid.

⁵The maximum spec limit for this parameter is equivalent to $I_{CC}(max)$ + 3 mA.



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

MAGNETIC CHARACTERISTICS over operating voltage and junction temperature range using reference target; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
		Switchpoint	-	7	_	bit
Number of Programming Bits		Switchpoint Polarity	_	1	_	bit
		Programming Lock	_	1	_	bit
Gear Tooth / Proximity Characteristics (Low switchpoint only)						
Programming Air Gap Range ¹ AG _R	10	Temperature = 25° C, Code = -127	2.5	-	-	mm
	AG _{Range}	Temperature = 25°C, Code = +127	-	-	1.5	mm
Programming Resolution	AG _{Res}	Temperature = 25°C Program Air Gap = 2.5 mm	-	0.05	-	mm
Air Gap Drift Over Full Temperature Range ²	AG _{Drift}	AG _{Drift} Device programmed to 2.5 mm		0.2	-	mm
Polarity	р	Over tooth (ATS636LSE)	-	Low	-	-
		Over valley (ATS636LSE)	_	High	_	_

¹The switchpoint will vary over temperature. A sufficient margin obtained through customer testing is required to guarantee functionality over temperature. Programming at larger air gaps leaves no safety margin for switchpoint drift. See the applications note *Proximity Sensing Programming Technique* on the Allegro website at http://www.allegromicro.com for additional information.

²The switchpoint will vary over temperature, proportionally to the programmed air gap. This parameter is based on characterization data and is not a tested parameter in production. Switchpoint air gap generally drifts downward as temperature increases.



Reference Target Flux Density vs. Position: Typical



Reference Target Tooth and Valley Field vs. Air Gap



Characteristic Performance

Data taken from 3 lots, 30 pieces/lot Reference Target 8x







7

6

5

4

3

2

1

0

-50

AIR GAP (mm)

Programmable Back Biased Hall-Effect Switch with TPOS Functionality

B_{OP}/B_{RP} vs. Program Code

Data taken from 3 lots, 30 pieces/lot Reference Target 8x

Notes:

• Air gaps for Code 127 at 150°C are interpolated due to test limitations at minimum air gap.

50

0

• These graphs are intended to provide an understanding of how the program codes affect the switchpoints. In a production environment, individual devices would be programmed to individual codes to ensure all devices switch at the same air gap.

TEMPERATURE (°C)

100

150



REFERENCE TARGET DIMENSIONS

Target	Outside Diameter	Face Width	Circular Tooth Length	Circular Valley Length	Tooth Whole Depth
	(D _o)	(F)	(T)	(P _C – T)	(h _t)
Reference Target	120 mm	6 mm	23.5 mm	23.5 mm	5 mm





Reference Target

Reference Target

Gear Parameters for Correct Operation

Characteristic	Description	Min.	Тур.	Max.	Unit
Tooth Whole Depth (h _t)	Depth of Target Valley	5	-	-	mm
Circular Valley Length (P _c – T)	Length of Target Valley	13	-	-	mm
Circular Tooth Length (T)	Length of Target Tooth	5	-	-	mm
Face Width (F)	Thickness or Width of Target Tooth	5	_	-	mm

Material: CRS 1018

Electromagnetic Capability (EMC) Performance

Please Contact Allegro MicroSystems for EMC Performance

Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-1
Direct RF Injection	ISO 11452-7
Bulk Current Injection	ISO 11452-4
TEM Cell	ISO 11452-3



Functional Description

Chopper-Stabilized Technique

The basic Hall element is a small sheet of semiconductor material in which a constant bias current will flow when a constant voltage source is applied. The output will take the form of a voltage measured across the width of the sheet and will have negligible value in the absence of a magnetic field. When a magnetic field with flux lines at right angles to the Hall current is applied, a small signal voltage directly proportional to the strength of the magnetic field will occur at the output terminals.

This signal voltage is proportionally small relative to the offset produced at the input of the chip. This makes it very difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Therefore, it is important to reduce any offset on the signal that could be amplified when the signal is processed.

Chopper stabilization is a unique approach used to minimize input offset on the chip. This technique removes a key source of output drift with temperature and stress, and produces a $3 \times$ reduction in offset over other conventional methods.

This offset reduction chopping technique is based on a signal modulation-demodulation process. The undesired offset signal is

separated from the magnetically induced signal in the frequency domain. The offset (and any low frequency noise) component of the signal can be seen as signal corruption added after the signal modulation process has taken place. Therefore, the DC offset is not modulated and remains a low frequency component. Consequently, the signal demodulation process acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high frequency signal. Then, using a low pass filter, the signal passes while the modulated DC offset is suppressed.

The advantage of this approach is significant offset reduction, which desensitizes the chip against the effects of temperature and stress. The disadvantage is that this technique features a demodulator that uses a sample and hold block to store and recover the signal. This sampling process can slightly degrade the signal-tonoise Ratio (SNR) by producing replicas of the noise spectrum at the baseband. The degradation is a function of the ratio between the white noise spectrum and the sampling frequency. The effect of the degradation of the SNR is higher jitter, a.k.a. signal repeatability. In comparison to a continuous time device, the jitter spec can be increased by a factor of five.



Figure 1. Concept of Chopper-Stabilization Algorithm



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Addressing / Programming Protocol

The ATS636LSE magnetic operate point, B_{OP} , is programmed by serially addressing the devices through the supply terminal (1). After the correct operate point is determined, the device programming bits are selected and blown, then a lock bit is selected and blown to prevent any further (accidental) programming.

Addressing B_{OP} is programmable in both the positive and negative direction from its initial value. Addressing is used to determine the desired code, while programming is used to lock the code. A unique key is needed to blow fuses, while addressing as described below does not allow for the device to be programmed accidentally.

Addressing with positive polarity The magnetic operate point, B_{OP} , is adjustable using 7 bits or 128 addresses. The addresses are sequentially selected (figure 2) until the required operate point is reached. The first address must be selected with a high voltage pulse, V_{PP} , while the remaining pulses should be V_{PH} pulses. Note that the difference between B_{OP} and the magnetic release point, B_{RP} , the hysteresis, B_{HYS} , is fixed for all addresses.

Addressing with negative polarity The magnetic operate point, B_{OP} , is adjustable with negative polarity using 7 bits or 128 addresses. To invert the polarity it is necessary to first apply a keying sequence (figure 3). The polarity key contains a V_{PP} pulse and at least 1 V_{PH} pulse, but no more than 6 V_{PH} pulses; the key in figure 3 shows 2 V_{PH} pulses. The addresses are then sequentially selected until the required operate point is reached. The first address must be selected with a high voltage pulse, V_{PP} , while the remaining pulses should be V_{PH} pulses.



Figure 2. Addressing Pulses: Positive Polarity



Figure 3. Addressing Pulses: Negative Polarity

PROGRAMMING PROTOCOL	Valid over operating temperature range,	unless otherwise noted
-----------------------------	---	------------------------

Characteristics	Symbol	Test Conditions		Тур.	Max.	Units
Programming Protocol (T _A = 25°C)						
	V _{PL}	Minimum voltage range during programming	4.5	5	5.5	V
Programming Voltage ^{1,2}	V _{PH}		8.5	-	15	V
	V _{PP}		25	-	27	V
Programming Current	I _{PP}	Maximum supply current during programming		500	_	mA
	t _{d(0)}	Off-time between bits	20	-	-	μs
Pulse Width	t _{d(1)}	Enable, address, program, or lock bit on-time	20	-	_	μs
	t _{dP}	Program pulse on-time	100	300	_	μs
Pulse Rise Time	t _r	V_{PL} to V_{PH} or V_{PP}	-	-	11	μs
Pulse Fall Time	t _f	V_{PH} or V_{PP} to V_{PL}	-	_	5	μs

 1 Programming voltages are measured at pin 1 (VCC) of the SIP. A minimum capacitance of 0.1 μ F must be connected from VCC to GND of the SIP to provide the current necessary to blow the fuse.

²Testing is the only method that guarantees successful programming.



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Program Enable To program the device, a keying sequence is used to activate / enable the programming mode as shown in figure 4. This program key sequence consisting of a VPP pulse, at least seven VPH pulses, and a VPP pulse with no supply interruptions. The sequence is designed to prevent the device from being programmed accidentally (e.g., as a result of noise on the supply line).

Code Programming After the desired switchpoint code is selected (0 through 127), each bit of the corresponding binary address should be programmed individually, not at the same time. For example, to program code 5 (binary 000101), bits 1 and

3 need to be programmed. A bit is programmed by addressing the code and then applying a V_{PP} pulse, the programming is not reversible. An appropriate sequence for blowing code 5 is shown in figure 5.

Polarity Bit Programming If the desired switchpoint has negative polarity, the polarity bit must be programmed. To do this it is necessary to first apply the polarity key sequence before the program key sequence (figure 6). Finally a V_{PP} pulse of duration t_{dP} must be applied to program this bit, the programming is not reversible. The polarity bit is for adjusting programming range only and will not affect the output polarity.



Figure 4. Program Enable Pulse Sequence





Figure 6. Polarity Bit Programming

Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Lock-Bit Programming After the desired code is programmed, the lock bit (code 128), can be programmed (figure 7) to prevent further programming of the device. Again, programming is not reversible. See Allegro website at http://www.allegromicro.com for extensive

information on device programming as well as programming products. Programming hardware is available for purchase and programming software is available for free.



Figure 7. Lock -Bit Programming Pulse Sequence



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Typical Application Circuit

For applications it is strongly recommended that an external ceramic bypass capacitor in the range of 0.01 μ F to 0.1 μ F be connected between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. (The diagram below shows a 0.1 μ F bypass capacitor.)

The series resistor R_S in combination with the bypass capacitor creates a filter for EMC pulses. The series resistor will have a drop of approximately 800 mV, this must be considered for the minimum V_{CC} requirement of the ATS636LSE. The small capacitor on the output of the device improves the EMC performance

of the device. The pull-up resistor should be chosen to limit the current through the output transistor; do not exceed the maximum continuous output current of the device.

Note: This circuit cannot be used to program the device, as the series resistance is too large, and a minimum capacitance of $0.1 \ \mu$ F must be connected from VCC to GND of the SIP to provide the current necessary to blow the fuse.

Extensive applications information on magnets and Halleffect ICs including chopper stabilization is available in the Allegro *Electronic Data Book* CD, or at the website: http://www.allegromicro.com.



Typical Application:



Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Power Derating – SE Package

Due to internal power consumption, the junction temperature of the IC (junction temperature, T_J) is higher than the ambient environment temperature, T_A . To ensure that the device does not operate above the maximum rated junction temperature use the following calculations:

$$\Delta T = P_D \times R_{aJA}$$

Where:

$$\begin{split} \mathbf{P}_{\mathrm{D}} &= \mathbf{V}_{\mathrm{CC}} \times \mathbf{I}_{\mathrm{CC}} \\ \mathbf{\Delta}\mathbf{T} &= \mathbf{V}_{\mathrm{CC}} \times \mathbf{I}_{\mathrm{CC}} \times \mathbf{R}_{\mathrm{qJA}} \end{split}$$

Where DT denotes the temperature rise resulting from the IC's power dissipation.

$$T_{J} = T_{A} + DT$$
$$R_{qJA} = 77^{\circ}C/W$$
$$T_{I}(max) = 165^{\circ}C$$

Typical T_J calculation:

$$\begin{split} T_{A} &= 25^{\circ}C \\ V_{CC} &= 5 V \\ I_{CC(on)} &= 5.5 \text{ mA} \\ P_{D} &= V_{CC} \times I_{CC} = 5 V \times 5.5 \text{ mA} = 27.5 \text{ mW} \\ DT &= P_{D} \times R_{qJA} = 27.5 \text{ mW} \times 77^{\circ}C/W = 2.0^{\circ}C \\ T_{J} &= T_{A} + DT = 25^{\circ}C + 2.0^{\circ}C = 27.0^{\circ}C \end{split}$$

Maximum Allowable Power Dissipation Calculation:

$$T_J = T_A + DT$$

 $T_J(max) = 165^{\circ}C, \text{ if } T_A = 150^{\circ}C$

then:

Maximum V_{CC} for $P_D(max) = 111$ mW at $T_A = 150^{\circ}C$

$$P_D = V_{CC} \times I_{CC}$$
, $I_{CC} = 10 \text{ mA (max) at } 150^{\circ}\text{C}$
 $V_{CC} = P_D / I_{CC} = 195 \text{ mW} / 5.5 \text{ mA} = 35.4 \text{ V}$

Power Dissipation versus Ambient Temperature





Package SE 4-Pin SIP





Programmable Back Biased Hall-Effect Switch with TPOS Functionality

Revision History

Revision	Revision Date	Description of Revision
5	January 30, 2012	Update product availability
6	December 1, 2015	Product status updated to discontinued

Copyright ©2005-2015, Allegro MicroSystems, LLC

Allegro MicroSystems, LLC reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website: www.allegromicro.com

