Document Number: MC100ES6017
Rev 2, 09/2005

3.3 V ECL/PECL Quad Differential Receiver

MC100ES6017

ECL/PECL QUAD DIFFERENTIAL RECEIVER

The MC100ES6017 is a 3.3 V ECL/PECL quad differential receiver. Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled down to V_{EE}. This operation will force the Q output LOW and ensure stability.

For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

- High bandwidth output transitions
- LVPECL operating range: V_{CC} = 3.0 V to 3.6 V
- Internal input pulldown resistors on D inputs, pullup and pulldown resistors on $\overline{D}$ inputs
- 20 lead SOIC package
- Ambient temperature range -40°C to +85°C
- 20-lead Pb-free package available

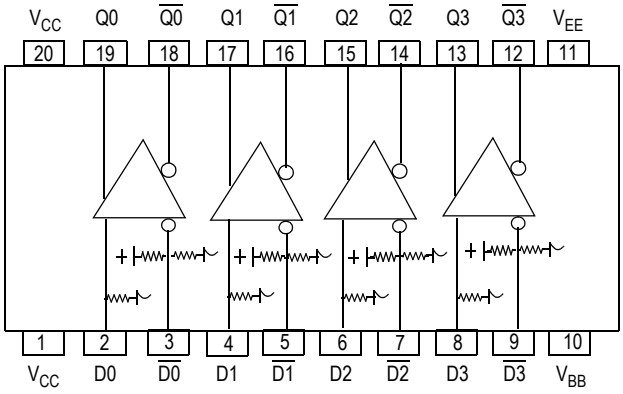


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-07

EG SUFFIX
20-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751D-07

ORDERING INFORMATION	
Device	**Package**
MC100ES6017DW	SO-20
MC100ES6017DWR2	SO-20
MC100ES6017EG	SO-20 (Pb-Free)
MC100ES6017EGR2	SO-20 (Pb-Free)

PIN DESCRIPTION	
Pin	**Function**
Dn, $\overline{D}$n	ECL Differential Data Inputs
Qn, $\overline{Q}$n	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	90 °C/W 60 °C/W
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	V_{CC} - V_{EE} ≤ 3.6 V	V_{CC} + 0.3 V_{EE} - 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
I_{BB}	V_{BB} Sink/Source		± 0.5	mA
TA	Operating Temp Range		-40 to +85	°C
T_{STG}	Storage Temp Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V or V_{CC} = 0 V; V_{EE} = -3.6 to -3.0 V)

		-40°C			0°C to 85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		20	31		28	35	mA
V_{OH}(1)	Output HIGH Voltage	V_{CC} - 1150	V_{CC} - 1020	V_{CC} - 800	V_{CC} - 1200	V_{CC} - 970	V_{CC} - 750	mV
V_{OL}(1)	Output LOW Voltage	V_{CC} - 1950	V_{CC} - 1620	V_{CC} - 1250	V_{CC} - 2000	V_{CC} - 1680	V_{CC} - 1300	mV
V_{IH}	Input HIGH Voltage	V_{CC} - 1165		V_{CC} - 880	V_{CC} - 1165		V_{CC} - 880	mV
V_{IL}	Input LOW Voltage	V_{CC} - 1810		V_{CC} - 1475	V_{CC} - 1810		V_{CC} - 1475	mV
V_{BB}(2)	Output Voltage Reference (I_{BB} = 0.5 mA)	V_{CC} - 1440		V_{CC} - 1235	V_{CC} - 1440		V_{CC} - 1235	mV
V_{PP}	Differential Input Votage	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage	V_{EE} + 1.3		V_{CC} - 0.9	V_{EE} + 1.3		V_{CC} - 0.9	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current $\underline{Dn}$ Dn	0.5 -300			0.5 -300			μA μA

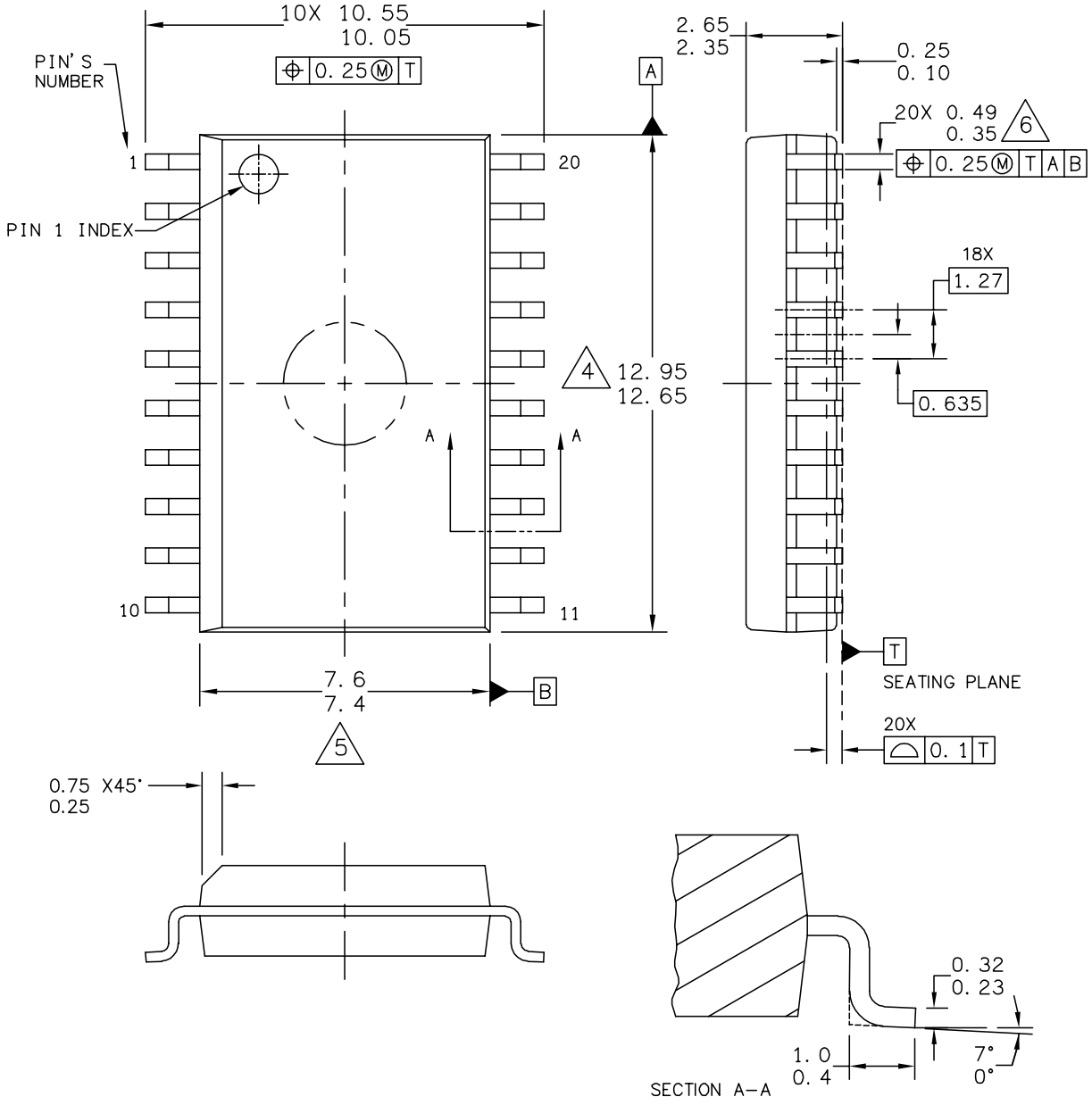
1. Outputs are terminated through a 50Ω resistor to V_{CC}-2 volts.
2. Input swing is centered around V_{BB}.

Table 4. AC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V or V_{CC} = 0 V; V_{EE} = -3.6 to -3.0 V)

Symbol	Characteristic	-40°C			25°C			85°C			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		1.75			1.75			1.75		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Diff S.E.(1)	310 225		510 595	310 225		510 595	310 225		510 595	ps
t_{SKEW}	Data Path Skew(2) (differential) Part-to-Part Skew(2) (differential) Pulse Width Skew (2) (3) (differential)			50 200 50			50 200 50			50 200 50	ps
t_{JITTER}	Cycle to Cycle Jitter			1			1			1	ps
V_{PP}(4)	Input Swing	150		1000	150		1000	150		1000	mV
t_r / t_f	Output Rise/Fall Times (20% - 80%)	50		250	50		250	50		250	ps

1. Single-ended input propagation delay requires t_r and t_f $\leq$ 350 ps to meet specified propagation delay. Device will function with larger t_r and t_f values.
2. Skews are valid across specified voltage range, part-to-part skew is for a given temperature and frequency
3. Pulse width skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
4. V_{PP} (min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of approximately 40.

PACKAGE DIMENSIONS



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	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

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CASE 751D-07
ISSUE J
20-LEAD SOIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	

CASE 751D-07
ISSUE J
20-LEAD SOIC PACKAGE

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