Reference Manual

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SPX-1

Eight Channel Analog Input Serial Peripheral Expansion (SPX™) Board and Development Kit

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Product Release Notes

Rev. 4

- Manufacturing improvements implemented.

Rev. 3

- Production release.

Rev. 2

- Beta Release.

Rev. 1

- Pre-production only. No customer releases.

Support Page

The SPX support page, at **http://www.versalogic.com/private/spx1support.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Data sheets and manufacturers' links for chips used in this product
- Utility routines and benchmark software

This is a private page for SPX users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

Table of Contents

Introduction 1

Description

The VersaLogic SPX-1 is an 8-channel analog input expansion module designed to be used with any SPX™ enabled base board. Its features include:

- National Semiconductor AD78H90 analog-to-digital converter
- Eight channels
- Compatible with any SPX enabled base board

VersaLogic SPX boards are a line of I/O expansion boards using the industry standard Serial Peripheral Interface (SPI) bus. These are small 1.2" x 3.775" that can mount in either "user connector" areas of a PC/104-*Plus* stack using the normal PC/104 stand-offs. They can also mount up to two feet away from the base board using custom cabling.

SPX boards are electrically connected to a base board via a 14-pin 2mm cable. Up to four boards can be daisy-chained together. Four is the maximum number of SPI chips that can be driven by the 14-pin interface. The SPI bus requires each chip to have a discrete chip-select signal, and the 14-pin interface supplies four chip-select signals. The maximum clock rate is 8 MHz.

Power for SPX boards is supplied through the interface cable.

I/O connections on SPX boards are provided through screw terminal/wire connections.

All SPX boards are RoHS compliant and industrial temperature rated.

ABOUT SPI

The SPI bus specifies four logic signals: SCLK – Serial clock (output from master); MOSI – Master output, slave input (output from master); MISO – Master input, slave output (output from slave); and SS – Slave select (output from master).

The SPI implementation on VersaLogic CPU boards adds additional features, such as hardware interrupt input to the master. The master initiates all SPI transactions. A slave device responds when its slave select is asserted and it receives clock pulses from the master.

Slave selects are controlled in one of two modes: manual or automatic. In automatic mode, the slave select is asserted by the SPI controller when the most significant data byte is written. This initiates a transaction to the specified slave device. In manual mode, the slave select is controlled by the user and any number of data frames can be sent. The user must command the slave select high to complete the transaction.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. All four common SPI modes are supported through the use of clock polarity and clock phase controls.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 1.2" x 3.775", SPX compliant
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
-40° C to +85° C
Power Requirements:
+5.0V ± 5% @ 9.4 mA (47 mW) typ.,
20 mA (100 mW) max.
(Interface cable provides 500 mA total, to be shared by SPX modules)
Analog Input:
8-channel, 12-bit, single-ended
Input range: 0 to +4.095V (1 mV per bit)
500 kSPS
Compatibility:
SPX – Full compliance
(Any 3.3V signaling SPI interface, 8 MHz maximum clock)
Weight:
0.034 lbs (0.015 kg)
Compliance:
RoHS – Full compliance

Specifications are subject to change without notice.

RoHS-Compliance

The SPX-1 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Technical Support

If you are unable to solve a problem with this manual please visit the SPX Product Support web page listed below. If you have further questions, contact VersaLogic technical support at (503) 747-2261. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

SPX Support Website

http://www.versalogic.com/private/spx1support.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. VersaLogic's standard turn-around time for repairs is five working days after the product is received.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contact if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

SPX-1 Board Layout

The figure below shows the dimensions of the SPX-1 board, as well as the location of connectors, jumpers, and mounting holes.

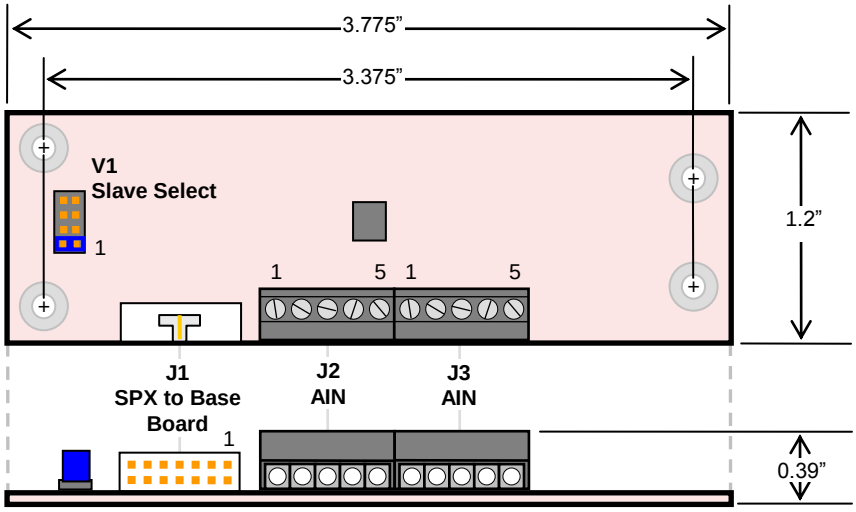

Figure 1. SPX-1 Board Layout
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The SPX-1 mounts on two hardware standoffs using the corner mounting holes. These standoffs are secured to the board, typically across the PC/104 and PC/104-*Plus* stack locations, using pan head screws, shown in Figure 2.

Standoffs and screws are available as part number VL-HDW-101.

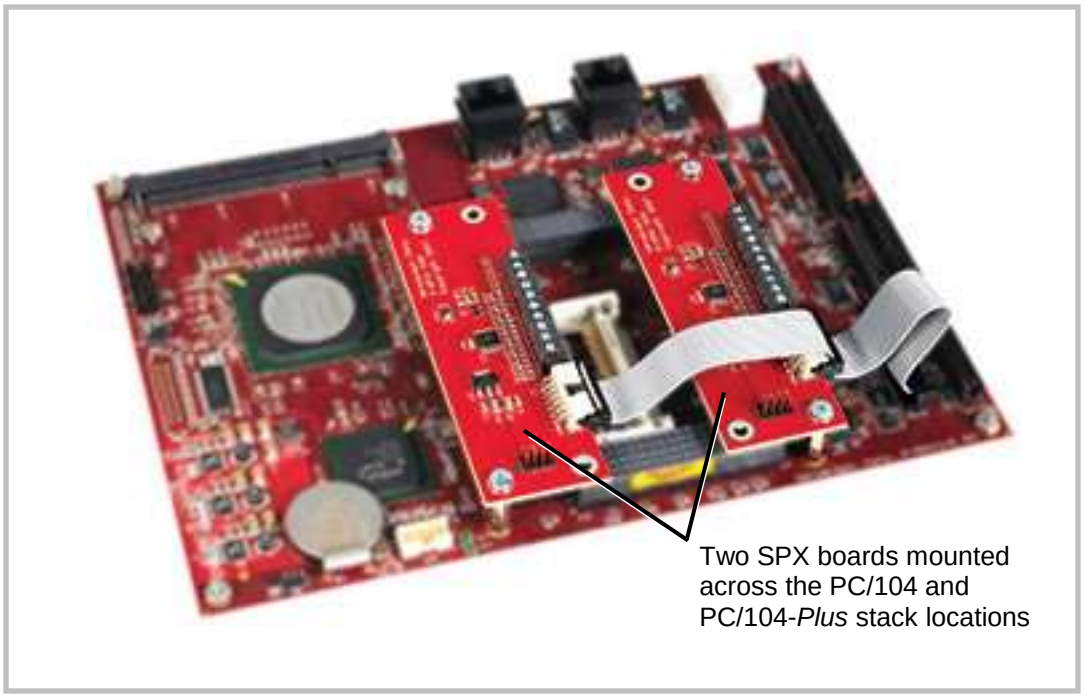

Figure 2. SPX Board Mounting

Connector Functions and Interface Cables

The following table shows the function of each connector, as well as mating connectors and cables.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description
J1	SPX to Base Board	FCI 89361-714LF or equivalent	CBR-1401 CBR-1402	2 SPX Module Cable 4 SPX Module Cable
J2	Analog Input	Bare wires to 5-pin screw terminal	–	–
J3	Analog Input	Bare wires to 5-pin screw terminal	–	–

Jumper Summary

Table 2: Jumper Summary

Jumper Block	Description	As Shipped
V1[1-2]	Slave Select 0	In
V1[3-4]	Slave Select 1	Out
V1[5-6]	Slave Select 2	Out
V1[7-8]	Slave Select 3	Out

J1 Connector Pinout

Table 3: J1 Connector Pinout

Pin	Signal Name	Description
1	V5_0	+5.0V
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Master In Slave Out
5	GND	Ground
6	MOSI	Master Out Slave In
7	GND	Ground
8	SS0#	Slave Select 0
9	SS1#	Slave Select 1
10	SS2#	Slave Select 2
11	SS3#	Slave Select 3
12	GND	Ground
13	SINT#	SPI Interrupt
14	V5_0	+5.0V

Analog Input 3

Description

The SPX-1 provides a multi-range, 12-bit A/D converter that accepts up to eight single-ended input signals. The converter features 500k samples per second, with input range of 0 to +4.095V.

The A/D converter communicates with the host computer through the SPX interface.

Note that the SPX-1 cannot be configured to issue an interrupt upon completion of an A/D conversion, so the software must poll the BUSY bit to determine when the conversion is complete.

External Connections

Single-ended analog voltages are applied to connectors J2 and J3 of the SPX-1 as shown in the following table.

Table 4: Analog Input Connectors

J2 Pin	Signal Name	Description
1	AIN1	Analog Input 1
2	AIN2	Analog Input 2
3	AIN3	Analog Input 3
4	AIN4	Analog Input 4
5	Ground	Ground
J3 Pin		
1	AIN5	Analog Input 5
2	AIN6	Analog Input 6
3	AIN7	Analog Input 7
4	AIN8	Analog Input 8
5	Ground	Ground

Calibration

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

ANALOG INPUT RANGE

Analog inputs are in binary format, 0 to +4.095V only.

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

Sample values are shown in the following table:

Table 5: Binary Data Format

0 to +5V Input Voltage	Hex	Decimal	Comment
>+4.095	–	–	Out of range
+4.095	0FFFh	4095	Maximum voltage
+2.048	0800h	2048	Half scale
+1.024	0400h	1024	Quarter scale
+0.001	0001h	1	1 LSB
0.000	0000h	0	Zero (ground input)

ANALOG CHANNEL SELECTION

Analog channel selection is controlled through the ADC Control Register within the ADC78H90 chip.

Table 6: ADC Control Register

D7	D6	D5	D4	D3	D2	D1	D0
–	–	ADC2	ADC1	ADC0	–	–	–

Table 7: ADC Channel Selection

ADC2	ADC1	ADC0	Input Channel
0	0	0	AIN1, J2 pin 1
0	0	1	AIN2, J2 pin 2
0	1	0	AIN3, J2 pin 3
0	1	1	AIN4, J2 pin 4
1	0	0	AIN5, J3 pin 1
1	0	1	AIN6, J3 pin 2
1	1	0	AIN7, J3 pin 3
1	1	1	AIN8, J3 pin 4

Initiating an Analog Conversion

The following procedure can be used to initiate an analog conversion.

1. Write 11h to the SPICONTROL register (I/O address 1D8h) – This value configures the SPI port to select external slave select 0 (SPX-1 default jumper setting), 16-bit frame length, low SCLK idle state, rising SCLK edge, and automatic slave select.
2. Write 30h to the SPISTATUS register (I/O address 1D9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.
3. Write any value to SPIDATA2 (I/O address 1DCh) – This data will be ignored by the A/D converter.
4. Write the analog input channel number to bits 5-3 of SPIDATA3 (1DDh) – Any write operation to this register triggers an SPI transaction.
5. Poll the BUSY bit until the conversion is completed.
6. Read the conversion data from SPIDATA2 (lower 8 bits) and SPIDATA3 (upper 4 bits).

Each analog conversion returns the conversion data from the previous conversion. The first analog conversion after power-up or reset returns the data from AIN1. The second conversion returns the conversion data from the channel addressed in the first conversion. Each successive conversion returns conversion data from the previous conversion.

This means that multiple conversions on the same A/D channel return valid data after every conversion, starting with the second conversion. However, if a different channel is selected between analog reads, two conversions will be necessary to return valid data from the new channel.

Analog Input Code Example

The following code example illustrates the procedure for reading an analog voltage from SPX-1 channel 3. A 32bit SPI frame is used to provide a valid single sample.

```
        MOV   DX, 1D8h
        MOV   AL, 31h      ;SPICONTROL: auto SS0#, 32bit frame, SCLK
                           ;idle low, rising edge active
        OUT   DX, AL
        MOV   DX, 1D9h
        MOV   AL, 30h      ;SPISTATUS: 8 MHz, no IRQ, left-shift data
        OUT   DX, AL
                           ;SPIDATA2, SPIDATA1, SPIDATA0: don't care
        MOV   DX, 1DDh
        MOV   AL, 10h      ;SPIDATA3: ADC78H90 AIN3 = SPX-1 AIN3
        OUT   DX, AL       ;Start conversion

BUSY:   MOV   DX, 1D9h
        IN    AL, DX       ;Get SPISTATUS
        AND   AL, 01h      ;Isolate the BUSY bit
        JNZ   BUSY         ;Loop back if conversion is not complete

        MOV   DX, 1DAh     ;Point to SPIDATA0 register
        IN    AX, DX       ;16bit input reads current conversion data
                           ;from SPIDATA1 into AH and from SPIDATA0 into
                           ;AL
```

For more detailed information on the EBX-11 A/D converter, please refer to the National Semiconductor ADC78H90 Datasheet.

Base Board SPI Registers

The following tables describe the SPI control and data registers of the EBX-11 Rev. 6.00 and later. This is the standard set of SPI registers for VersaLogic CPU boards with an SPX interface. See the reference manual for details and updates.

SPICONTROL (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 8: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 9: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts.
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPI DATA REGISTERS

SPIDATA0 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1DBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1DCh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.