CONNOR WINFIELD

THE CONNOR-WINFIELD CORP.
2111 COMPREHENSIVE DRIVE.
AURORA, IL 60505.
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PRODUCT DATA SHEET

CRYSTAL CONTROLLED OSCILLATORS

CLOCK SMOOTHER MODULE
CSA2 - Series

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-55	-	125	°C	
Supply Voltage	(Vcc)	0	-	6.0	Vdc	
E/D and DS Input Voltage	(Vi)	0	-	6.0	Vdc	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Output Frequency	(Fo)	-	-	800	MHz	
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	80	100	mA	
Jitter (BW=10Hz to 20MHz)		-	-	3.0	ps rms	
Jitter (BW=12kHz to 80MHz)		-	-	0.5	ps rms	
SSB Phase Noise at 100Hz offset		-	-70	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-105	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-145	-	dBc/Hz	
SSB Phase Noise at 100KHz offset		-	-155	-	dBc/Hz	

REFERENCE INPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Input Frequency Range		19.44	-	200	Vdc	
Input Frequency Voltage		0.370	-	1.125	V pk to pk	1
Tracking Capability - Frequency Range Absolute Pull Range (APR)		+/-50	-	-	ppm	
Monotonic Linearity		-10	-	10	%	

CMOS INPUT CHARACTERISTICS (DS1, DS2, ENABLE / DISABLE)

TABLE 4.0

PARAMETER			MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Enable Input Voltage	(Low)	(Vi)	-	-	0.8	Vdc	2
Disable Input Voltage	(High)	(Vi)	2.0	-	-	Vdc	2
Divider Select Input Voltage	(Low)	(Vi)	-	-	0.8	Vdc	3
Divider Select Input Voltage	(High)	(Vi)	2.0	-	-	Vdc	3

LOW VOLTAGE PECL OUTPUT CHARACTERISTICS

TABLE 5.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	4
Voltage (High)	(Voh)	2.275	-	-	Vdc	
Voltage (Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle at 50% Level		45	50	55	%	
Rise / Fall Time measured 20% to 80%		-	120	500	pS	

PACKAGE CHARACTERISTICS

TABLE 6.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.

PROCESS RECOMMENDATIONS

TABLE 7.0

Solder Reflow	The component solder used internal to this device has a melting point of 221°C. The peak temperature inside the device should be less than or equal to 220°C for a maximum of 10 seconds
Wash	Ultrasonic cleaning is not recommended.

Notes
1.0 CMOS input signal requires attenuation to the 1000 mV level.
2.0 When oscillator is disabled the true output is in a low state (Vol) and the complementary output is in the high state (VoH)
3.0 Default divider ratio, no connection DS1 and DS2 is divide by 32.
4.0 50 ohm termination into Vcc-2V or Thevein equivalent.

FEATURES

- Jitter smoothing PLL utilizing a VCSO (Voltage Controlled SAW Oscillator).
- 1000mV Pk-to-Pk Input Reference Signal
- LVPECL Differential Outputs.
- Jitter Transfer: OC-192 (Telcordia GR-253) Compliant.
- Very low jitter generation.
- Low Phase Noise.
- Locked to specific input frequencies from 19.44MHz to 200MHz.
- Selectable Frequency divider.
- Divide by Ratios: 4, 8, 16 or 32.
- Lock detect monitor.
- Output Frequencies up to 800MHz.
- 3.3Vdc single supply voltage.
- Small SMT Package: 14.22mm x 11.68mm x 3.56mm, 10 Pins.

APPLICATIONS

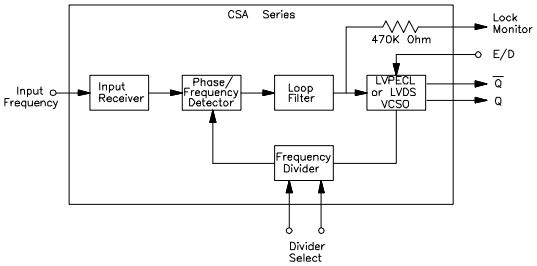
- SONET/SDH
- Clock Smoothing

ORDERING INFORMATION *

CSA21 - 622.08 MHz

Module Series — Center Frequency

* See Table 8



Specifications subject to change without notice.

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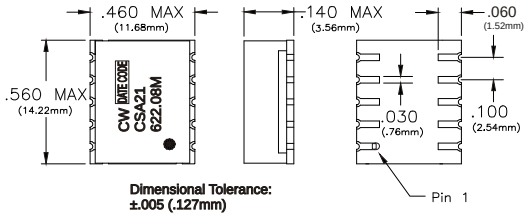
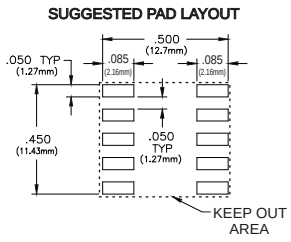




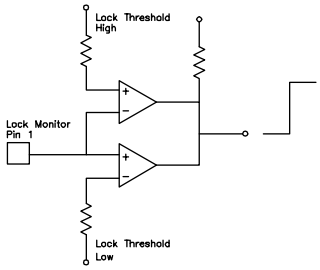


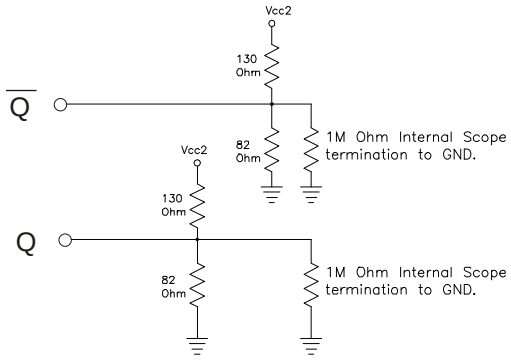
TABLE 8.0

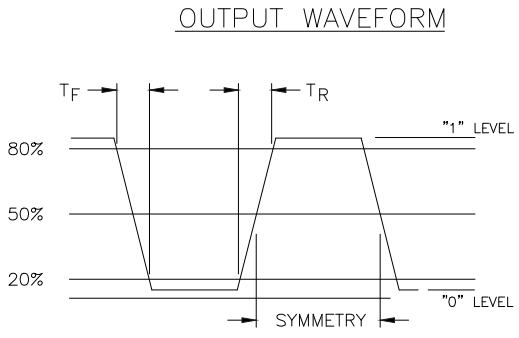
Model Number	Input Frequency	Divider	Output Frequency	Output Logic
CSA21	19.44 MHz	32	622.08 MHz	LVPECL
CSA21	38.88 MHz	16	622.08 MHz	LVPECL
CSA21	77.76 MHz	8	622.08 MHz	LVPECL
CSA21	155.52 MHz	4	622.08 MHz	LVPECL
CSA22	20.916456 MHz	32	669.3266 MHz	LVPECL
CSA22	41.832912 MHz	16	669.3266 MHz	LVPECL
CSA22	83.665825 MHz	8	669.3266 MHz	LVPECL
CSA22	167.331650 MHz	4	669.3266 MHz	LVPECL

Pin	Function
1	Lock Monitor
2	Enable / Disable
3	DS1
4	Ground (Case)
5	Reference Clock Input
6	DS2
7	Comp Output
8	Q Output
9	Ground (Case)
10	Vcc

Divider Select		
DS1	DS2	Divider Ratio
LOW	LOW	4
HIGH	LOW	8
LOW	HIGH	16
HIGH	HIGH	32

LVPECL TERMINATION DIAGRAM





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