D2SS28081XH25AA

Specifications

Density:	1GB	**Data Rate:**	800 Mbps
Version:	Unbuffered	**CAS Latency:**	6
Package:	SO-DIMM	**Votage:**	1.8V
Pin Count:	200pin	**PCB Layers:**	6
Speed:	PC2-6400	**ECC :**	Non ECC
Component Config:	128Meg x 8	**Module Ranks :**	Singel Rank

Features

- All of Lead-Free products are compliant for RoHS
- 200-pin,small outline,dual in-line memory module(SO-DIMM)
- 1.8V ± 0.1V power supply
- Data rate:800Mbps(max)
- 8 Banks
- JEDEC standard 1.8V I/O(SSTL_18-compatible)
- Burst Length: 4,8
- /CAS Latency (CL):3,4,5,6
- Double-data-rate architecture: two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- Four-bit prefetch architecture
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- Differential data strobe(DQS,DQS#) option
- DLL to align DQ and DQS transitions with CK
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Posted CAS# additive latency (AL)
- On Die Termination (ODT)
- 64ms,8192-cycle refresh
- Serial presence detect with EEPROM
- Gold edge contacts
- Average Refresh Period
  7.8us at 0℃ ≦TCASE≦＋85℃,
  3.9us at＋ 85℃ ＜TCASE≦＋95℃

D2SS28081XH25AA

Description

The D2SS28081XH25AA is 128M words x 64 bits, 1 ranks DDRII SDRAM Small Outline Dual In-line Memory Module, mounting 8 pieces of 1GB bits DDRII SDRAM sealed in FBGA(μBGA®) package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 4 bits prefetch-pipelined architecture. Data strobe (DQS and /DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop(DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each FBGA(μBGA) on the module board.

Speed Grade & Key Parameters

	DDR2-533	DDR2-667	DDR2-800	Unit
CL3	400	400		Mbps
CL4	533	533	533	Mbps
CL5		667	667	Mbps
CL6			800	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	tCK

Speed Bins

	DDR2-533	DDR2-667	DDR2-800	Unit
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	
Parameter	min	min	min	
CAS Latency	4	5	6	tCK
tRCD	15	15	15	ns
tRP	15	15	15	ns
tRAS	45	45	45	ns
tRC	60	60	60	ns

Address Configuration

	256MB	512MB	512MB	1GB	1GB	2GB
Dram Organization	32Mx16	64Mx8	64Mx16	64Mx8	128Mx8	128Mx8
Row address	A0~A12	A0~A13	A0~A12	A0~A13	A0~A13	A0~A13
Column address	A0~A9	A0~A9	A0~A9	A0~A9	A0~A9	A0~A9
Auto Precharge	A10	A10	A10	A10	A10	A10
Bank address	BA0~BA1	BA0~BA1	BA0~BA2	BA0~BA1	BA0~BA2	BA0~BA2
Refresh Method	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms
# of DRAMs	4	8	4	16	8	16

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
DRAM Component Case Temperature Range	T_{CASE}	0 to 95	℃	1
Storage Temperature	T_{STG}	-50 to +100	℃	
Storage Humidity	H_{STG}	5 to 95	%	

Note:

1. If the DRAM case temperature is above 85℃，the AUTO-Refresh command interval has to be reduced to tREFI=3.9us。

DC Operating Conditions(SSTL_1.8)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VDD	1.7	1.8	1.9	V
	VDDL	1.7	1.8	1.9	V
	VDDQ	1.7	1.8	1.9	V
Reference voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
Termination voltage	VTT	VREF – 0.04	VREF	VREF +0.04	V
Input high voltage	VIH	VREF + 0.15	-	VREF + 0.30	V
EEPROM Supply Voltage	VDDSPD	1.7	-	3.6	V
DC input logic high	V_{IH}(DC)	V_{REF}+0.125	-	V_{DDQ}+0.3	V
DC input low	V_{IL}(DC)	-0.3		V_{REF}-0.125	V
AC input logic high	V_{IH}(AC)	V_{REF}+0.250	-	-	V
AC input low	V_{IL}(AC)	-	-	V_{REF}-0.250	V

D2SS28081XH25AA

Pin Description

Pin name	Description	Pin name	Description
A0~A13	DDR2 SDRAM address bus	CK0,CK1	Clock input
BA0,BA1	DDR2 SDRAM bank select	/CK0,/CK1	Differential clock input
/RAS	DDR2 SDRAM row address strobe	SCL	Clock input for serial PD
/CAS	DDR2 SDRAM column address strobe	SDA	Data input/output for serial PD
/WE	Wirte enable	SA0-SA1	Serial address input
S0,S1	DIMM Rank Select Lines	VDD*	DDR2 SDRAM core power supply
CKE0,CKE1	DDR2 SDRAM clock enable lines	VDDQ*	DDR2 SDRAM I/O Driver power supply
ODT0,ODT1	On-die termination control lines	VREF	Input reference supply
DQ0-DQ63	DIMM memory data bus	VSS	Ground
CB0-CB7	DIMM ECC check bits	VDDSPD	Power for serial EEPROM
DQS0-DQS8	DDR2 SDRAM data strobes	NC	No connect
DM(0-8)	DDR2 SDRAM data masks	RESET	Not used on UDIMM
DQS0-DQS8	DDR2 SDRAM differential data strobes	TEST	Unused on memory DIMMs

Pin Configuration

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VSS	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	VSS	4	DQ4	53	VSS	54	VSS	103	VDD	104	VDD	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	VSS	156	VSS
7	DQ1	8	VSS	57	DQ19	58	DQ23	107	BA0	108	RAS	157	DQ48	158	DQ52
9	VSS	10	DM0	59	VSS	60	VSS	109	WE	110	S0	159	DQ49	160	DQ53
11	DQS0	12	VSS	61	DQ24	62	DQ28	111	VDD	112	VDD	161	VSS	162	VSS
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	CAS	114	ODT0	163	NC,TEST	164	CK1
15	VSS	16	DQ7	65	VSS	66	VSS	115	NC/S1	116	A13	165	VSS	166	CK1
17	DQ2	18	VSS	67	DM3	68	DQS3	117	VDD	118	VDD	167	DQS6	168	VSS
19	DQ3	20	DQ12	69	NC	70	DQS3	119	NC/ODT1	120	NC	169	DQS6	170	DM6
21	VSS	22	DQ13	71	VSS	72	VSS	121	VSS	122	VSS	171	VSS	172	VSS
23	DQ8	24	VSS	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	VSS	28	VSS	77	VSS	78	VSS	127	VSS	128	VSS	177	VSS	178	VSS
29	DQS1	30	CK0	79	CKE0	80	NC/CKE1	129	DQS4	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	CK0	81	VDD	82	VDD	131	DQS4	132	VSS	181	DQ57	182	DQ61
33	VSS	34	VSS	83	NC	84	NC	133	VSS	134	DQ38	183	VSS	184	VSS
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	DQS7
37	DQ11	38	DQ15	87	VDD	88	VDD	137	DQ35	138	VSS	187	VSS	188	DQS7
39	VSS	40	VSS	89	A12	90	A11	139	VSS	140	DQ44	189	DQ58	190	VSS
41	VSS	42	VSS	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	VSS	193	VSS	194	DQ63
45	DQ17	46	DQ21	95	VDD	96	VDD	145	VSS	146	DQS5	195	SDA	196	VSS
47	VSS	48	VSS	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	DQS2	50	NC	99	A3	100	A2	149	VSS	150	VSS	199	VDDSPD	200	SA1

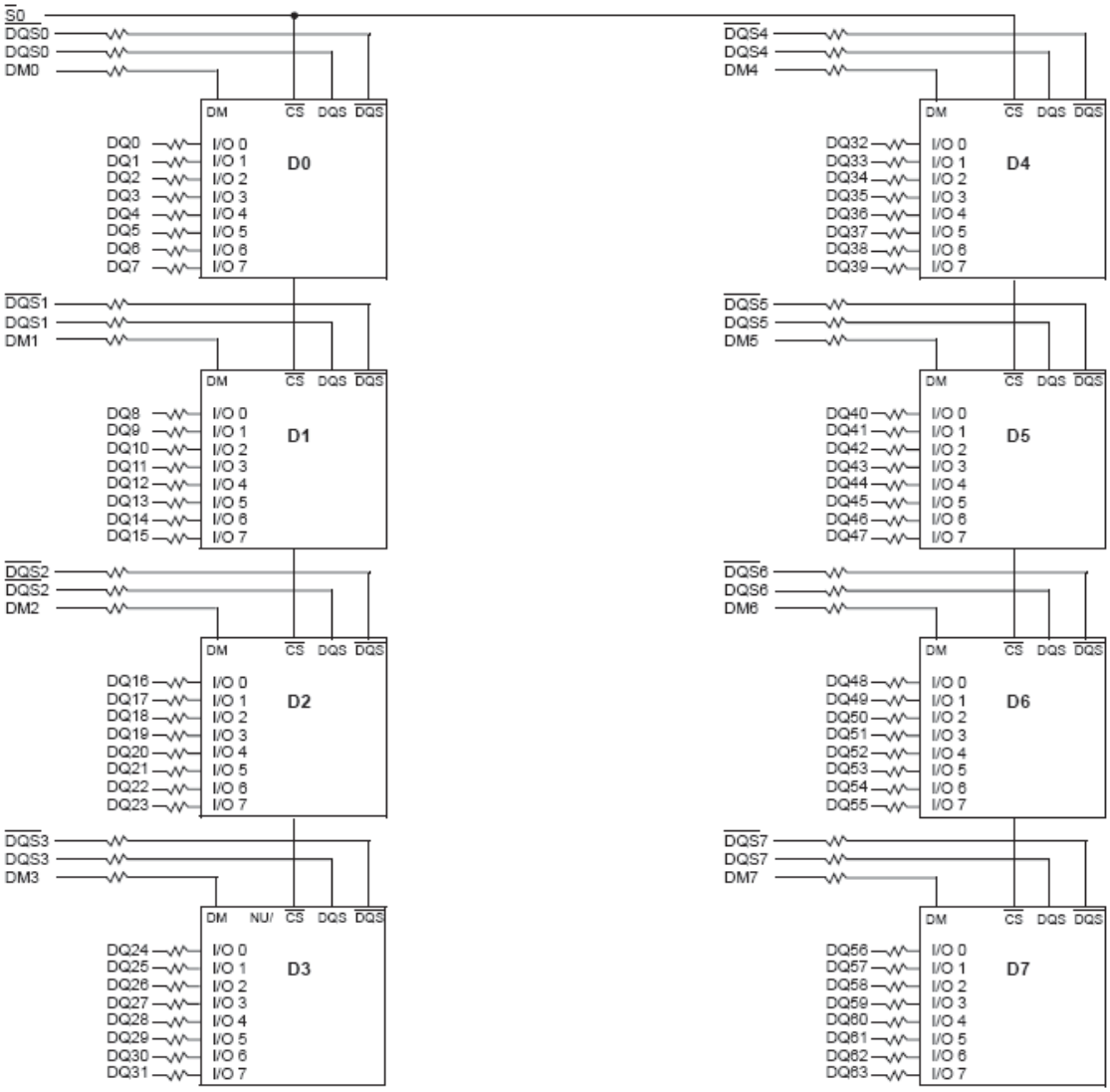
Input/Output Functional Description

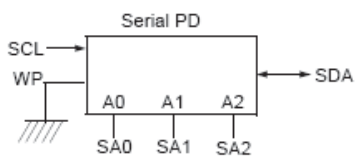
Symbol	Type	Function
CK0-CK2 CK0-CK2	Input	CK and /CK are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing)
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clock, CKE low initiates the Powe Down mode, or the Self-Refresh mode.
/S0-/S1	Input	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
/RAS,/CAS,/WE	Input	/RAS,/ CAS, and /WE(ALONG WITH CS) define the command being entered.
ODT0-ODT1	Input	When high, termination resistance is enabled for all DQ, /DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
VREF	Supply	Reference voltage for SSTL 18 Inputs.
VDDQ	Supply	Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR 2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA1	Input	Selects which SDRAM BANK of four is activated.
A0-A13	Input	During a Bank Activate command cycle, Address input defines the row address(RA0-RA13) During a Read or Write command cycle. Address input defines the column address. In addition to the column address. AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1 are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	In/Out	Data and Check Bit Input/Output pins.
DM0-DM8	Input	DM is and input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
VDD, VSS	Supply	Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
DQS0-DQS8 DQS0-DQS8	In/Out	Data strobe for input and output data. For Rawcards using x16 organized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM
SA0-SA2	Input	These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EERPOM address range.
SDA	In/Out	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup on the system board.
VDD SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 1.7V to 3.6V.

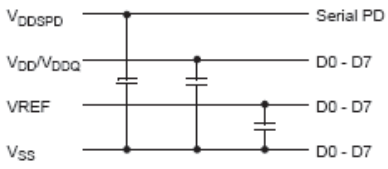
D2SS28081XH25AA

FUNCTIONAL BLOCK DIAGRAM

(Populated as 1 rank of x8 DDR2 SDRAMs)







* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA2 → BA0-BA2 : DDR2 SDRAMs D0 - D7
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
RAS → RAS : DDR2 SDRAMs D0 - D7
CAS → CAS : DDR2 SDRAMs D0 - D7
CKE0 → CKE : DDR2 SDRAMs D0 - D7
WE → WE : DDR2 SDRAMs D0 - D7
ODT0 → ODT : DDR2 SDRAMs D0 - D7

Note :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	+450	-400	+400	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	+400	-350	+350	ps	
CK high-level width	tCH	0.45	0.55	0.48	0.52	tCK	
CK low-level width	tCL	0.45	0.55	0.48	0.52	tCK	
CK half period	tHP	min(tCL, tCH)	-	min(tCL, tCH)	-	ps	
Clock cycle time, CL=x	tCK	3000	8000	2500	8000	ps	
DQ and DM input setup time (differential strobe)	tDS	100	-	50	-	ps	1
DQ and DM input hold time (differential strobe)	tDH	175	-	125	-	ps	1
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max		tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	-	240	ps	
DQ hold skew factor	tQHS	-	340	-	300	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	-0.25	+0.25	-0.25	+0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Address and control input setup time	tIS	200	-	175	-	ps	
Address and control input hold time	tIH	275	-	250	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Activate to precharge command	tRAS	45	70000	45	70000	ns	
Row Active to Row Active Delay for 1KB page size	tRRD	7.5	-	7.5	-	ns	
Row Active to Row Active Delay for 2KB page size	tRRD	10	-	10	-	ns	
Four Active Window for 1KB page size products	tFAW	37.5	-	35	-	ns	
Four Active Window for 2KB page size products	tFAW	50	-	45	-	ns	

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2	-	tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK	
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5	-	ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	tRFC + 10	-	ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2	-	2	-	tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL	-	8 - AL	-	tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3	-	3	-	tCK	
ODT turn-on delay	tAOND	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	-	3	-	tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	-	tIS+tCK+tIH	-	ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

Notes:

1. For details and notes, please refer to the relevant Hynix component datasheet(HY5PS1G8(16)31CFP).

2. $0°C \leq T_{CASE} \leq 85°C$

3. $85°C < T_{CASE} \leq 95°C$

D2SS28081XH25AA

SERIAL PRESENCE DETECT

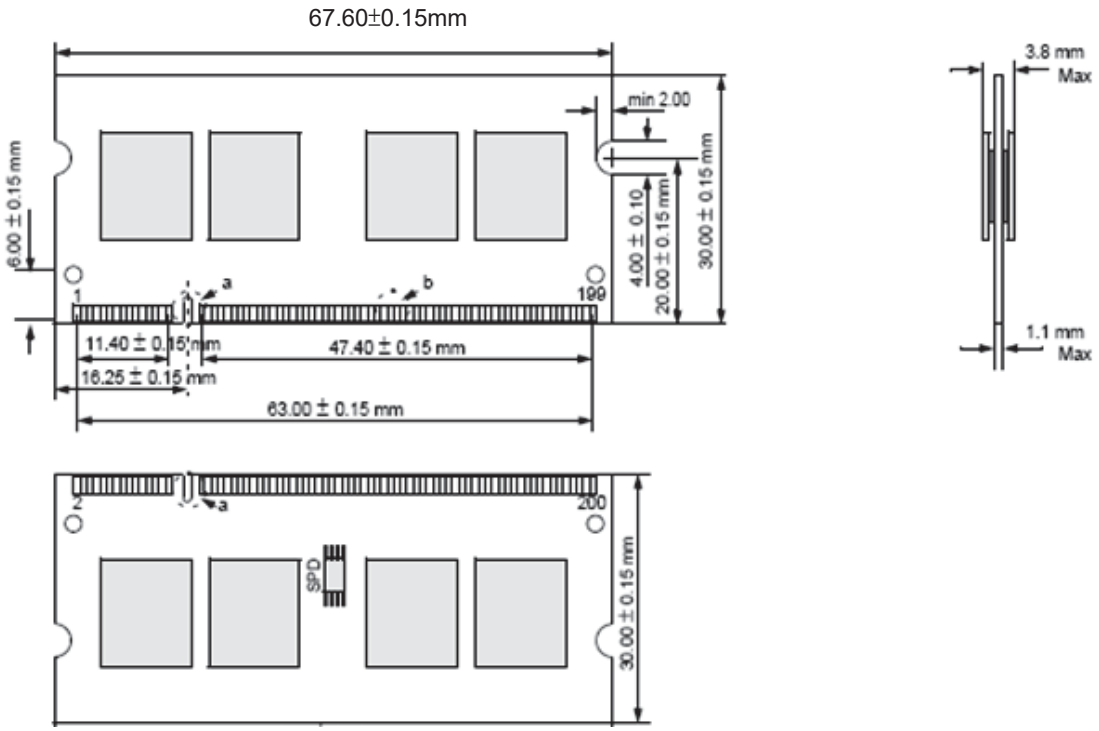
Byte No.	Function Described	Function Supported	Hex Value
0	# of Serial PD Bytes written during module production	128 Bytes	80
1	Total number of Bytes in SPD device	256 Bytes	08
2	Fundameatal memory type	DDR2 SDRAM	08
3	# of row address on this assembly	14	0E
4	# of column address on this assembly	10	0A
5	# of module rows on this assembly	1 rank	60
6	Data width of this assembly	64bits	40
7	Reserved	--	00
8	Voltage interface level of this assembly	SSTL 1.8V	05
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	2.5ns	25
10	DDR2 SDRAM Access time from clock at CL=X	4.0ns	40
11	DIMM configuration type(address&command parity, data parity,ECC)	Non parity/ECC	00
12	Refresh rate	7.8us	82
13	Primary DDR2 SDRAM width	X8	08
14	Error checking DDR2 SDRAM width	N/A	00
15	Reserved	--	00
16	DDR2 SDRAM device attributes:Burst lengths supported	4,8	0C
17	DDR2 SDRAM device attributes:# of banks on each DDR2 SDRAM Device	4	08
18	DDR2 SDRAM device attributes: CAS latency supported	4,6,6	70
19	Reserved		01
20	DIMM type information	SO-DIMM	04
21	DDR2 SDRAM module attributes	--	00
22	DDR2 SDRAM device attributes : General	50ohm ODT	07
23	DDR2 SDRAM cycle time at CL = X-1	3.75ns	30
24	DDR2 SDRAM access time from clock at CL = X-1	0.45ns	45
25	DDR2 SDRAM cycle time at CL = X-2	3.75ns	3D
26	DDR2 SDRAM access time from clock at CL = X-2	0.5ns	50
27	Minimum row precharge time(=tRP)	15ns	3C
28	Minimum row active to row active delay(=tRRD)	7.5ns	1E
29	Minimum RAS to CAS delay(=tRCD)	15ns	32
30	Minimum active precharge time(=tRAS)	45ns	2D

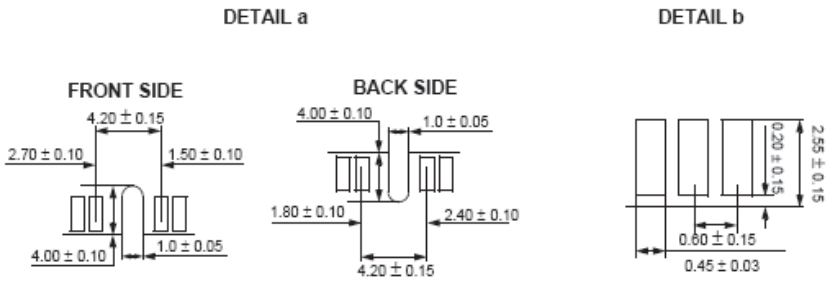
Byte No.	Function Described	Function Supported	Hex Value
31	Module rank density	1GB	01
32	Command and address setup time before clock(=tIS)	0.17ns	17
33	Command and address hold time after clock(=tIH)	0.25ns	25
34	Data input setup time before strobe(=tDS)	0.05ns	05
35	Data input hold time after strobe(=tDH)	0.12ns	12
36	Write recovery time (tWR)	15ns	3C
37	Write to read CMD delay (tWTR)	7.5ns	1E
38	Read to precharge CMD delay (tRTP)	7.5ns	1E
39	Mem analysis probe	TBD	00
40	Extension of byte 41 and 42	Undefined	06
41	Active command period (tRC)	60ns	3C
42	Auto refresh to active/ Auto refresh command cycle (tRFC)	105ns	7F
43	SDRAM tCK cycle max (tCK max)	8ns	80
44	Dout to DQS skew	0.20ns	14
45	Data hold skew (tQHS)	0.30ns	1E
46	PLL relock time	Undefined	00
47 to 61	Reserved	--	--
62	SPD data revision code	Revision 1.0	12
63	Checksum for Bytes 0~ 62	--	E2
64 to 94	Manufacturer JEDEC ID code	--	
95 to 98	Assembly serial #	--	
99 to 127	Manufacturer specific data(may be used in future)	Undefined	
128 to 225	Open for customer use	Undefined	

D2SS28081XH25AA

PACKAGE DIMENSIONS

Unit:mm





The used device is SAMSUNG, 128M x 8 ,FBGA

DDR2 SDRAM Part No.: K4T1G084QG-BCF7 *8EA

Declaration of Compliance with the RoHS Directive

DATA SPECIALTIES CO.,LTD. Hereby declares that the products compliant with the European Union Directive 2002/95/EC for Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment(RoHS Directive).

Below list of DSL(DATA SPECIALTIES CO.,LTD.) products are Compliance.

No.	Substance	Max. Conc.
1	Cd (Cadmium)	<100ppm
2	Hg (Mercury)	<1000ppm
3	Pb (Lead)	<1000ppm
4	Cr+6 (Hexavalent Chromium)	<1000ppm
5	PBB (Polybrominated Biphenyl ethers)	<1000ppm
6	PBDE (Polybrominated Diphenyl)	<1000ppm

DSL Lead-free products don't contain intentionally the prohibited substances above.
And the substances are controlled under the limit as impurity.

DATA SPECIALTIES CO., LTD.
Approved: Quality Engineering Team
Issued Date: 2007-06-20
Doc. No.: DS-20070620-1-0

Declaration of Compliance with the REACH Directive

Data Specialties Co. Ltd. hereby declares that the products described not contain the 16 SVHCs(substances of very high concern) and Cyclododecane(CAS no.294-62-2). SVHCs are defined by REACH Article 57 and in accordance with Directive 67/548/EEC and criteria set out in REACH Annex XIII. These 16 substances will be included in the 'Candidate List. Cyclododecane, the Member State Committee (MSC)unanimously agreed that there was no sufficient scientific data to justify identification under Article 57.

No.	Substance Name	CAS number	Content below 0.1%
1	Anthracene	120-12-7	Yes
2	4,4'- Diaminodiphenylmethane	101-77-9	Yes
3	Dibutyl phthalate (DBP)	84-74-2	Yes
4	Cyclododecane	294-62-2	Yes
5	Cobalt dichloride	7646-79-9	Yes
6	Diarsenic pentaoxide	1303-28-2	Yes
7	Diarsenic trioxide	1327-53-3	Yes
8	Sodium dichromate	7789-12-0	Yes
9	5-tert-butyl-2,4,6-trinitro-m-xylene(musk xylene)	81-15-2	Yes
10	Bis (2-ethyl(hexyl)phthalate)(DEHP)	117-81-7	Yes
11	Hexabromocyclododecane(HBCDD)	25637-99-4	Yes
12	Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins)	85535-84-8	Yes
13	Bis(tributyltin)oxide(TBTO)	56-35-9	Yes
14	Lead hydrogen arsenate	7784-40-9	Yes
15	Benzyl butyl phthalate (BBP)	85-68-7	Yes
16	Triethyl arsenate	15606-95-8	Yes

Note: REACH (Registration,Evaluation,Authorization and Restriction of Chemicals, EC 1907/2006) is the European Union's (EU) chemical substances regulatory framework, REACH requires manufactory to provide customers with sufficient information on Substances of Very high concern (SVHC) contained in products in concentration above 0.1% weight by weight (W/W) to allow safe use of the product.

DATA SPECIALTIES CO., LTD.
Approved: Quality Engineering Team
Issued Date: 2009-11-20
Doc No: DS-20091120-1-0

Declaration of Compliance with the PFOS Directive

DATA SPECIALTIES CO.,LTD . Hereby declares that the products we supply is compliant with DIRECTIVE 2006/122/ECOF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL regarding exception of the use in photoresist or anti reflective coatings for photolithigrahy(usually semiconductor).

DATA SPECIALTIES CO., LTD.

Approved: Quality Engineering Team

Issued Date: 2008-07-01

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