Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0292.

Devices Connected/Referenced			
AD7176-2	24-Bit, 250 kSPS, Σ-Δ ADC with 20 µs Settling	AD8475	Precision, Selectable Gain, Fully Differential Funnel Amplifier
ADR4550	Ultralow Noise, High Accuracy, 5.0 V Voltage Reference	ADuM3471	Isolated Switching Regulators (3/1 Channel Directionality)
ADA4096-4	30 V, Micropower, Overvoltage Protection, RRIO, Quad Op Amp	ADP7102	20 V, 300 mA, Low Noise, CMOS LDO Regulator
ADG1204	Low Capacitance, Low Charge Injection, *i*CMOS®, ±15 V/±12 V, 4:1 Multiplexer	ADA4898-1	High Voltage, Low Noise, Low Distortion, Unity Gain Stable, High Speed Op Amp
ADP1720	50 mA, High Voltage, Micropower Linear Regulator	ADP7182	−28 V, 200 mA, Low Noise, Linear Regulator

Completely Isolated, Robust, 4-Channel, Multiplexed Data Acquisition System for Industrial Level Signals

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0292 Circuit Evaluation Board (EVAL-CN0292-SDZ)
System Demonstration Platform, SDP-B (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a completely isolated, robust, industrial, 4-channel data acquisition system that provides 16-bit, noise free code resolution and an automatic channel switching rate of up to 42 kSPS. The channel to channel crosstalk at 42 kSPS switching is less than 15 ppm FS (less than −90 dB) because of the unique selection of fast settling components in the multiplexed signal chain.

The circuit acquires and digitizes standard industrial signal levels of ±5 V, ±10 V, 0 V to 10 V, and 0 mA to 20 mA. The input buffers also provide overvoltage protection, thereby eliminating the leakage errors associated with conventional Schottky diode protection circuits.

Applications for the circuit include process control (PLC/DCS modules), battery testing, scientific multichannel instrumentation, and chromatography.

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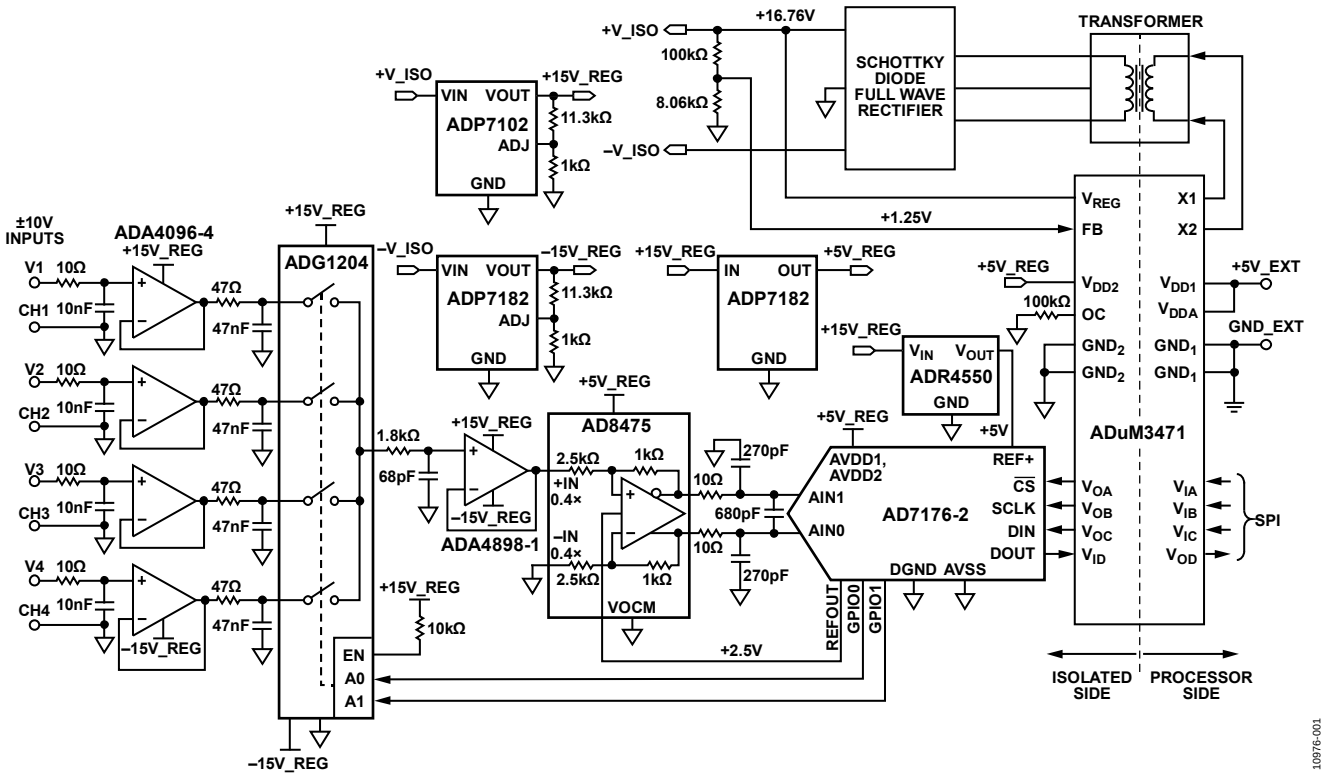

Figure 1. Functional Block Diagram of 4-Channel Data Acquisition System (Simplified Schematic: All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

Signal Path

Four channels of input signals are buffered by the ADA4096-4, a quad, rail-to-rail, input/output op amp featuring overvoltage protection against phase reversal or latch-up for inputs of up to 32 V above or below the ±15 V supply rails, which eliminates the need for additional overvoltage protection circuitry.

The inputs are designed for typical low frequency, industrial signals of ±10 V. The input buffers provide a high impedance to the sources and isolate the inputs from the multiplexer switching transients.

The RC networks on the inputs of the buffers (10 Ω/10 nF) have a bandwidth of 1.6 MHz and provide high frequency noise filtering.

The RC networks on the outputs of the ADA4096-4 (47 Ω/47 nF) isolate the buffers from the multiplexer switching transients. Figure 2 shows an equivalent circuit. The drain capacitor, C_D, must be charged by the input voltage before switching to the next channel. There can be as much as 20 V between channels, and a transient current is generated when the multiplexer switches to the next channel.

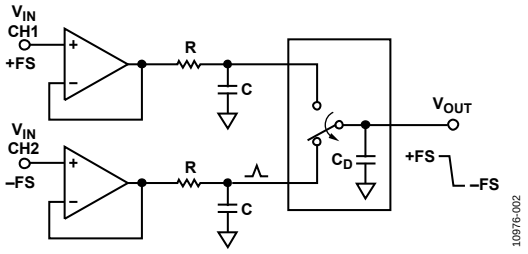

Figure 2. RC Kickback Isolation Circuit

The ADG1204 multiplexer, featuring low drain capacitance (<4 pF), minimizes the kickback charge.

The output of the multiplexer is buffered by an ADA4898-1 op amp to prevent loading errors due to the on resistance of the switches. The ADA4898-1 is unity-gain stable, settles to 0.1% in less than 85 ns, and has only 0.9 nV/√Hz of input voltage noise. The worst-case input signal to the buffer is a ±10 V, 21 kHz square wave when two adjacent channels have full-scale positive and full-scale negative voltages on their respective inputs.

The RC network on the input of the ADA4898-1 (1.8 kΩ/68 pF) has a bandwidth of 1.3 MHz and acts as a wideband noise filter. The time constant of this filter is 122 ns, and the 16-bit settling time is achieved in approximately 1.34 µs (~11 time constants).

The output of the ADA4898-1 buffer drives the AD8475 precision differential funnel amplifier that converts the bipolar, single-ended ±10 V signal into a ±4 V differential signal centered on a common-mode voltage of 2.5 V. With integrated, trimmed, and matched precision resistors configured to a gain of 0.4×, the AD8475 can accept up to ±12.5 V inputs operating on a single 5 V supply. The common-mode voltage is supplied by the REFOUT pin (2.5 V) of the AD7176-2 ADC.

The differential input range of the AD7176-2 is set to ±5 V by the ADR4550 5 V reference.

The AD7176-2 operates both as an ADC and as a multiplexer controller. Enabling the MUX_IO bit causes the GPIO pins in the AD7176-2 to toggle in synchronization with the sequencing and conversion of the ADC channels; therefore, the channel change is synchronized with the ADC, eliminating any need for external synchronization. The GPIO pins save two control lines to the digital interface that are otherwise needed to control the multiplexer.

A programmable conversion delay from 0 µs to 1 ms can be configured in the AD7176-2. The conversion delay is the delay between each channel change (controlled by the GPIO bits) and the start of a conversion. The delay adjustment allows the multiplexer and conditioning circuits additional settling time.

All the components in the signal path were selected to provide a total minimum settling time that is compatible with the channel switching rate of 42 kSPS. The resulting low frequency crosstalk between channels for full-scale signals is less than −90 dB.

A programmable conversion delay can be inserted between channel switching and start of conversion, thereby allowing maximum settling time for the circuits driving the ADC if further optimization is required.

Digital Isolation and isoPower

The ADuM3471 is a quad channel digital isolator with integrated pulse-width modulation (PWM) controllers and low impedance transformer drivers (X1 and X2). The only additional components required for an isolated dc-to-dc converter are a transformer (Coilcraft KA4976-AL, 1:5 turns ratio, 64 µH primary inductance) and a simple full-wave Schottky diode rectifier (four SD103AW-7-F diodes). The power circuit provides up to 2 W of regulated, isolated power when supplied from a 5 V or 3.3 V input, thereby eliminating the need for a separate isolated dc-to-dc converter.

The *i*Coupler® chip-scale transformer technology isolates the logic signals, and the integrated transformer driver with isolated secondary side control provides high efficiency for the isolated dc-to-dc converter. The internal oscillator frequency is adjustable from 200 kHz to 1 MHz and is determined by the value of a resistor connected to the OC pin. When the resistor is 100 kΩ, the switching frequency is 500 kHz.

The ADuM3471 regulation is from the positive supply. The feedback for regulation is from a divider network chosen such that the feedback voltage is 1.25 V when the output voltage is 16.76 V. The feedback voltage is compared with the ADuM3471 internal feedback set point of 1.25 V. Regulation is achieved by varying the duty cycle of the PWM signal driving the external transformer.

The ADP7102 LDO regulator regulates the 16.76 V output voltage down to 15 V. The negative unregulated rectified voltage from the transformer is approximately −21 V. The ADP7182 negative regulator is used to provide the regulated −15 V. The regulated ±15 V is then used to power the high voltage components (the ADA4096-4, ADG1204, and ADA4898-1).

Performance Measurements

Noise Free Code Resolution

With the channel input shorted to GND, the circuit measured 17-bit noise free code resolution as shown in Figure 3.

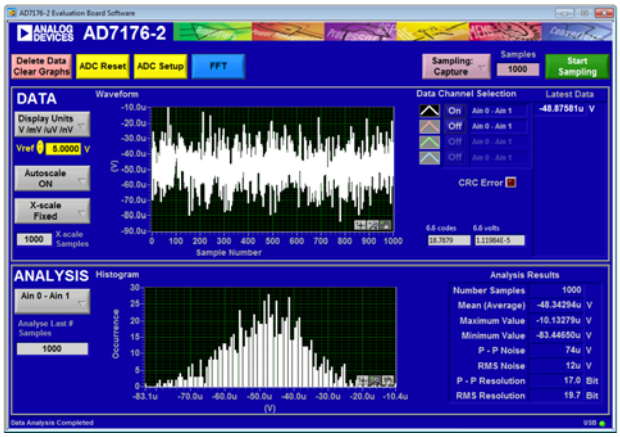

Figure 3. Noise and Resolution at 42 kSPS Switching

Settling when Multiplexing Between Channels

A 9.6 V source (battery pack) was connected to the system as the input for Channel 1 and Channel 3. A −9.6 V source was connected to Channel 2 and Channel 4.

The multiplexer was manually set to Channel 1 by setting the GPIO bits to 00, and a histogram of 1000 samples was obtained as shown in Figure 4. The noise free code resolution was better than 16 bits.

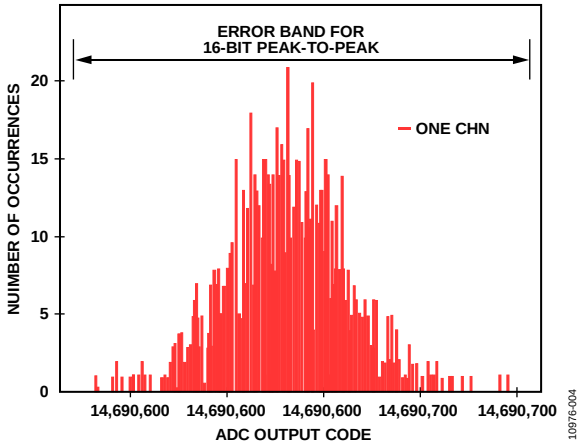

Figure 4. Histogram of Single Channel 9.6 V Conversion

The multiplexer was then enabled (42 kSPS at 4 µs delay), and a histogram of 1000 samples was obtained for Channel 1 as shown in Figure 5. The noise free code resolution was better than 16 bits.

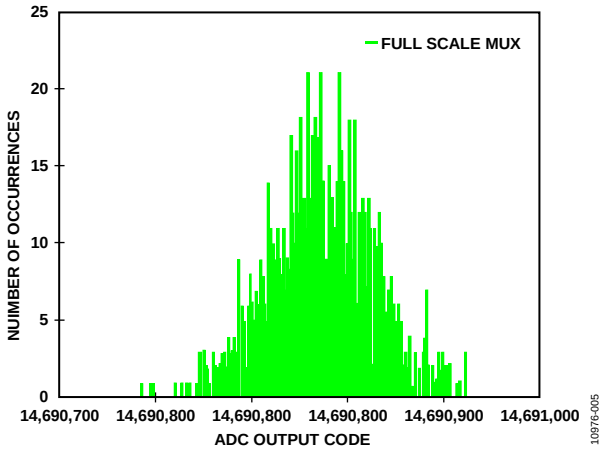

Figure 5. Histogram of Channel 1 Conversion with Multiplexer Switching Between +9.6 V and −9.6 V at 42 kSPS (4 µs Conversion Delay)

Each configuration resulted in better than 16-bit, noise free code resolution, with a slight offset shift in the mean value when multiplexing between channels as shown in Figure 6. The shift is approximately 300 µV (15 ppm FS, or 1 LSB at 16 bits) at 42 kSPS, and can be reduced by adding more conversion delay (configured in the ADC mode register of the AD7176-2) and thereby allowing more settling time before conversions.

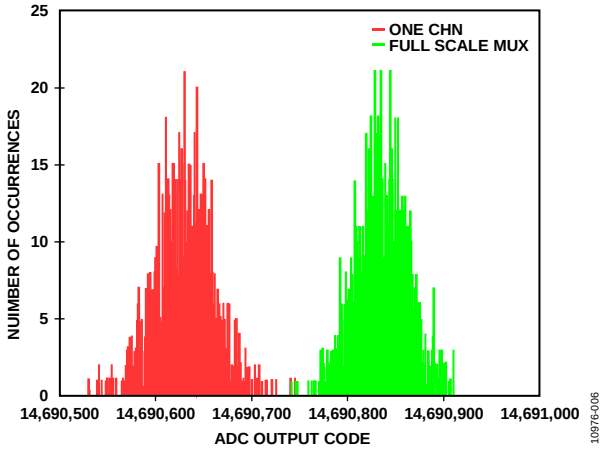

Figure 6. Histogram of Channel 1 Conversion with and without Multiplexing

Integral Nonlinearity

Integral nonlinearity (INL) was measured from −11 V to +11 V in 1 V steps using a Fluke 5700 multifunction calibrator and an Agilent 3458 multimeter.

The results are shown in Figure 7, where the endpoint linearity error is calibrated to zero.

The AD7176-2 has a typical INL specification of ±3 ppm FS. Other devices on the board also introduce nonlinearity but not all of them peak at the same voltage, resulting a U shape curve, as shown in the Figure 7.

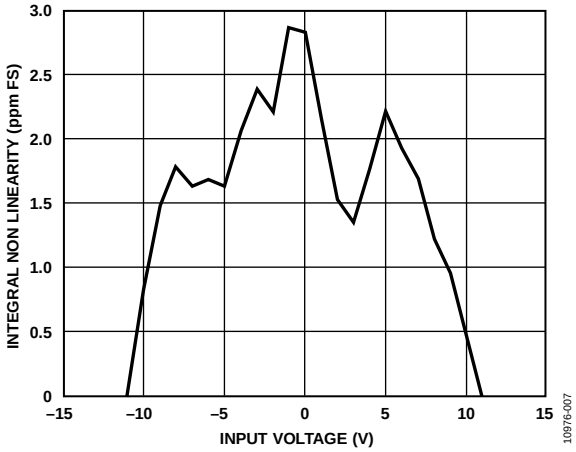

Figure 7. INL in ppm of FSR vs. Input Voltage

With the default values in calibration registers, offset and gain error calculated from −11 V and +11 V were 318 µV and 0.04% FS, respectively, at 25°C.

Table 1 shows the contribution from each device to the offset and gain drift over temperature.

Table 1. Offset and Gain Drift Contributions

Part No.	Offset Drift	Gain Drift
ADA4096-4	0.4 µV/°C	Not applicable
ADA4898-1	0.4 µV/°C	Not applicable
AD8475	2.5 µV/°C	1 ppm/°C
AD7176-2	110 nV/°C	0.5 ppm/°C
ADR4550	Not applicable	2 ppm/°C (maximum)
RSS Value	2.56 µV/°C	2.29 ppm/°C
Maximum Value	3.41 µV/°C	3.5 ppm/°C

A complete design support package including the schematics, layout, assembly, and bill of materials used in the CN-0292 is available in the CN-0292 Design Support Package.

COMMON VARIATIONS

4 mA to 20 mA Input Configuration

By connecting the voltage inputs to ground with 499 Ω resistors, the circuit operates as a 4-channel, 0 mA to 20 mA, single-ended input. Because the full-scale signal is approximately half of the ADC range, the dynamic range of the system is reduced by 1 bit. The input can be reconfigured for current inputs by making the appropriate external connections to Connector J2.

For example, in the voltage mode for Channel 1, the voltage is applied to Terminal 1 of J2, and the ground to Terminal 3. In the current mode, the current is applied to Terminal 1 and Terminal 2, and the ground to Terminal 3.

Table 2. Connections to J2 for Voltage and Current Input Options

Input	Voltage Mode Input Terminals	Current Mode Input Terminals
Channel 1	1, 3 (GND)	1 and 2, 3 (GND)
Channel 2	4, 6 (GND)	4 and 5, 6 (GND)
Channel 3	7, 9 (GND)	7 and 8, 9 (GND)
Channel 4	10, 12 (GND)	10 and 11, 12 (GND)

±5 V Input Configuration

In the Figure 1 circuit, the 0.4× gain configuration of the AD8475 was chosen. If the 0.8× gain option is chosen, the full-scale range is reduced from ±10 V to ±5 V, yielding twice the sensitivity. The 0.8× gain option also allows full utilization of the ADC input range when using a 4 mA to 20 mA input and a 250 Ω termination resistor.

Achieving Wider Bandwidth

The input bandwidth can be increased by changing the input buffers to the ADA4000-4 and reducing the second stage input filter capacitors. Distortion performance when measuring ac signals also improves significantly.

Scaling the Design to 8 Channels

A second channel consisting of a buffer, multiplexer, and attenuator can be connected to the AN2/AN3 input of the AD7176-2 ADC to achieve 8-channel operation. However, no more than four channels at a time can be automatically sequenced; therefore, running the ADC in single conversion mode and reconfiguring the channel mapping once every four channel conversions is recommended.

The AD7173-8 has a 4-bit GPIO and is capable of sequencing between 16 channels of the external multiplexer. The AD7173-8 is slower (6.21 kSPS channel switching) but consumes less power than the AD7176-2.

CIRCUIT EVALUATION AND TEST

Equipment Required

The following equipment is required:

- The EVAL-CN0292-SDZ evaluation board
- The EVAL-SDP-CB1Z system demonstration platform
- The CN-0292 Evaluation Software
- A 5 V at 1 A dc power source, or wall wart
- A precision dc voltage source (Fluke 5700)
- A digital multimeter (Agilent 3458)
- A low noise, precision voltage source (a battery pack is recommended)
- A PC running Windows® XP (SP2), Windows Vista, or Windows 7 (32-bit or 64-bit) with USB port

Software Installation

A complete software user guide can be found in the CN-0292 User Guide.

The CN-0292 evaluation kit requires self installing software that can be downloaded from ftp://ftp.analog.com/pub/cftl/CN0292/. The software is compatible with Windows XP (SP2), Windows Vista, and Windows 7 (32-bit or 64-bit). If the setup file does not automatically run, run **setup.exe** from the file.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After the evaluation software installation is complete, connect the EVAL-SDP-CB1Z (via either Connector A or Connector B) to the EVAL-CN0292-SDZ and then connect the EVAL-SDP-CB1Z to the USB port of the PC using the supplied cable.

When the evaluation system is detected, proceed through any dialog boxes that appear to complete the installation.

Setup and Test

A functional block diagram of the test setup is shown in Figure 8.

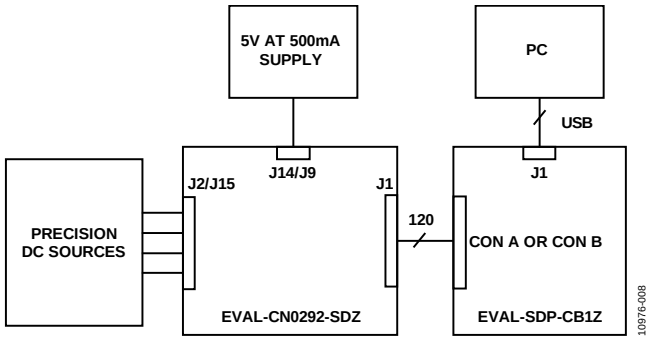

Figure 8. Test Setup Function Diagram

The following hardware configuration is required to test the circuit:

- Set all links on the EVAL-CN0292-SDZ board to the default Position A (this configures the board to be powered by *iso*Power® and LDO for ±15 V and 5 V supplies).
- Power the board with a dc 5 V, 1 A power source connected to J14 (see Figure 10).
- Connect ±10 V single-ended signals to V1 through V4 on Connector J2.

The following ADC software configuration is recommended for optimized performance:

1. Enable **GPIO Mux**.
2. Set **Delay Conversion** to 4 µs.
3. Enable **Data + Status**.
4. Enable the channels that are to be measured.
5. Choose the external reference.
6. Leave other registers as reset value.
7. To select the channel manually, disable **GPIO Mux**, enable **GPIO 0 Output** and **GPIO 1 Output**, and set the channel number on **GPIO 0 Data** and **GPIO 1 Data**.

The test setup is now configured (see Figure 9). Set the number of samples to 1000, and then click **Start Sampling**.

When the samples are gathered, the results display in the main waveform graph. Note that the voltage reading are referred to ADC inputs; therefore, a 10 V input on J2/J15 results in an approximate 4 V reading in the software.

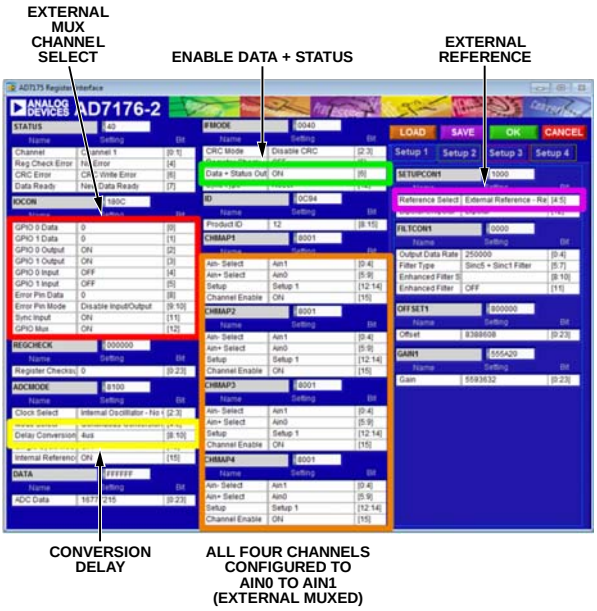

Figure 9. ADC Configuration for 4-Channel Multiplexed Conversion at 42 kSPS

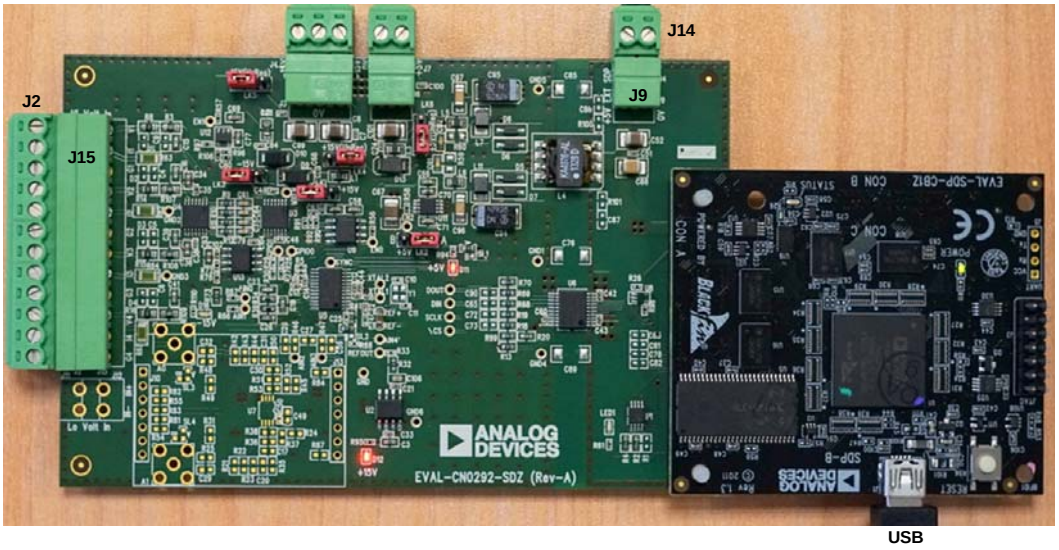

Figure 10. Photo of EVAL-CN0292-SDZ Evaluation Board Connected to EVAL-SDP-CB1Z SDP Board

LEARN MORE

CN-0292 Design Support Package.

Pachchigar, Maithil. *Demystifying High-Performance Multiplexed Data-Acquisition Systems.* Analog Dialogue 48-07, July 2014.

Kester, Walt. "Multichannel Data Acquisition Systems" in *The Data Conversion Handbook,* Section 8-2. Analog Devices/ Elsevier, 2005.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*. Analog Dialogue 39-09, September 2005.

MT-004 Tutorial. *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial. *ADC Architectures III: Sigma-Delta ADC Basics.* Analog Devices.

MT-023 Tutorial. *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-074 Tutorial. *Differential Drivers for Precision ADCs.* Analog Devices.

MT-075 Tutorial. *Differential Drivers for High Speed ADCs Overview*. Analog Devices.

MT-076 Tutorial. *Differential Driver Analysis*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

MT-088 Tutorial. *Analog Switches and Multiplexers Basics.* Analog Devices.

UG-478. *Evaluation Board for the AD7176-2—24-Bit, 250 kSPS Sigma-Delta ADC with 20 µs Settling*. Analog Devices.

Data Sheets and Evaluation Boards

AD7176-2 Data Sheet

ADR4550 Data Sheet

ADA4096-4 Data Sheet

ADG1204 Data Sheet

ADA4898-1 Data Sheet

AD8475 Data Sheet

ADuM3471 Data Sheet

ADP7102 Data Sheet

ADP1720 Data Sheet

ADP7182 Data Sheet

REVISION HISTORY

11/14—Revision 0: Initial Version