

# PMDPB65UP

20 V, 3.5 A dual P-channel Trench MOSFET

Rev. 2 — 8 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin SOT1118 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Trench MOSFET technology
- 1.8 V  $R_{DSon}$  rated for low voltage gate drive
- 1 kV ElectroStatic Discharge (ESD) protection
- Small and leadless ultra thin SMD plastic package: 2 × 2 × 0.65 mm
- Exposed drain pad for excellent thermal conduction

### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disk and computing power management

### 1.4 Quick reference data

Table 1. Quick reference data

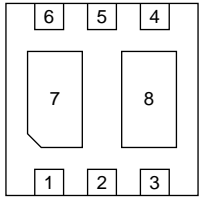
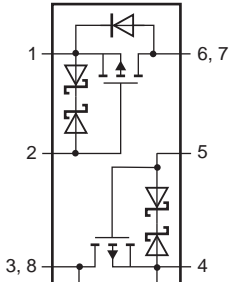
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-3.5	A
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -1\text{ A};$ $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01;$ $T_j = 25\text{ °C}$	-	58	70	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source 1	 <p>Transparent top view <b>SOT1118 (HUSON6)</b></p>	 <p>017aaa062</p>
2	G1	gate 1		
3	D2	drain 2		
4	S2	source 2		
5	G2	gate 2		
6	D1	drain 1		
7	D1	drain 1		
8	D2	drain 2		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
PMDPB65UP	HUSON6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code
PMDPB65UP	1C

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

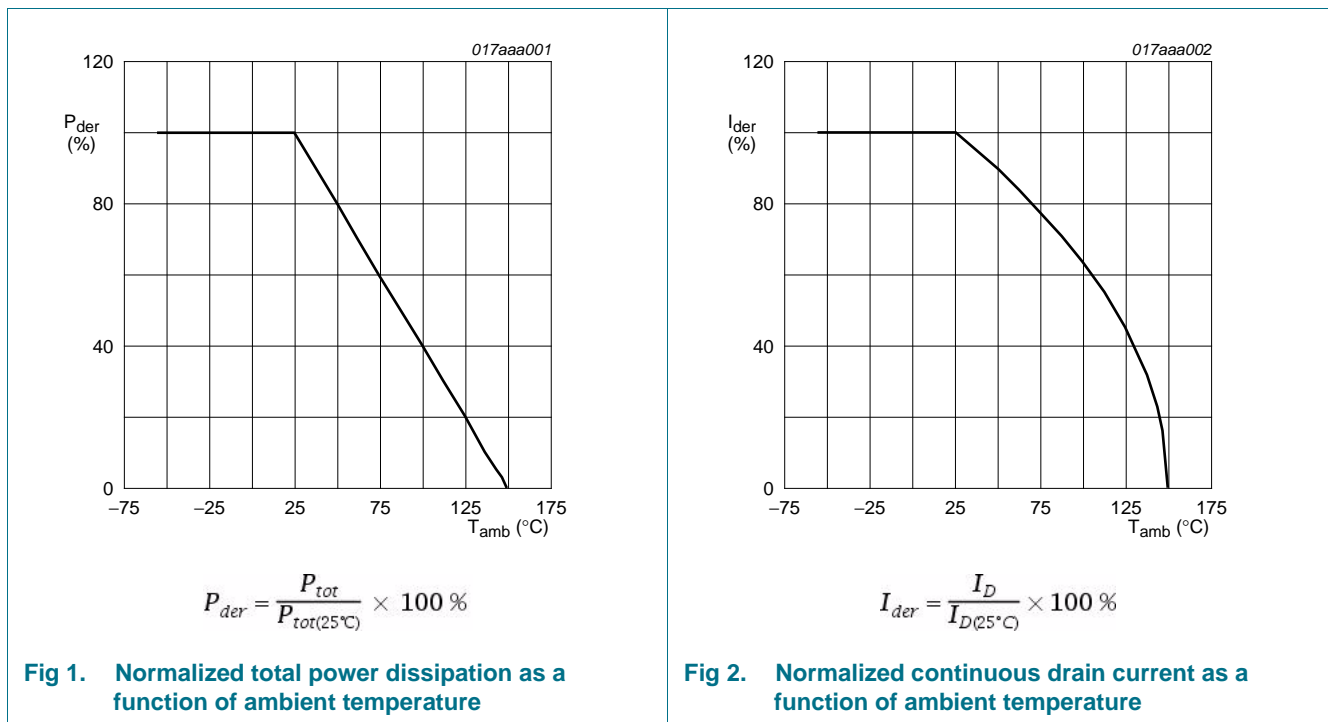
Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-20	V	
$V_{GS}$	gate-source voltage		-8	8	V	
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-3.5	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-2.7	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-20	A	
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	520	mW
			[1]	-	1.25	W
		$T_{sp} = 25\text{ °C}$		-	8.3	W

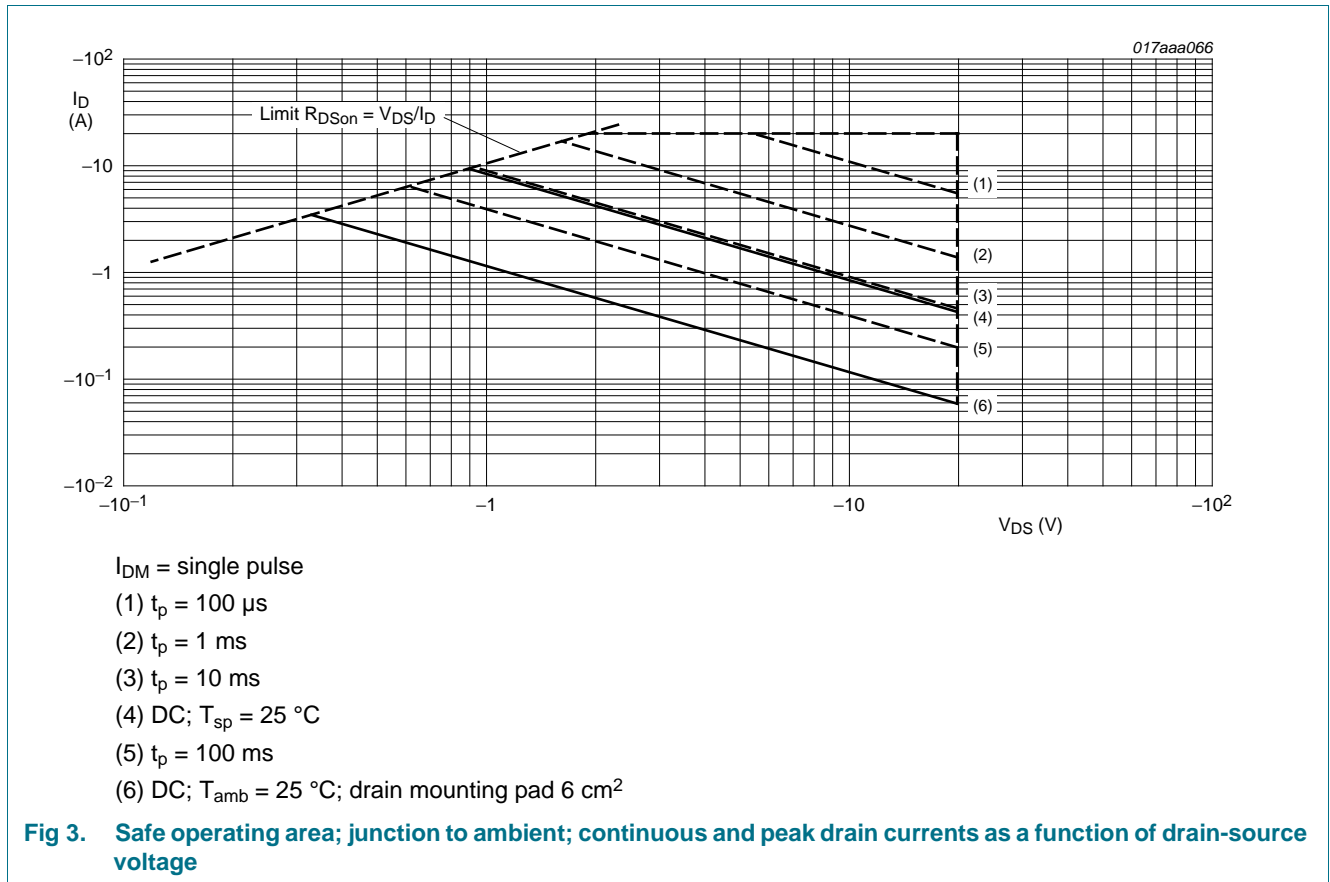
**Table 5. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per device</b>					
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	150	°C
T <sub>stg</sub>	storage temperature		-65	150	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-1.4	A
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	1000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	240	K/W
			[2]	-	-	100	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ .

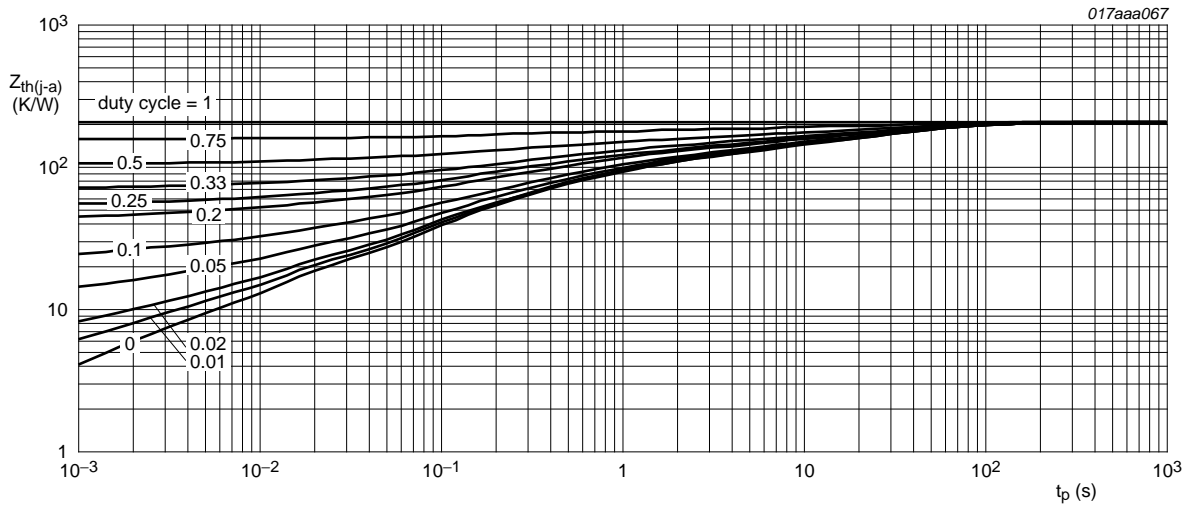


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

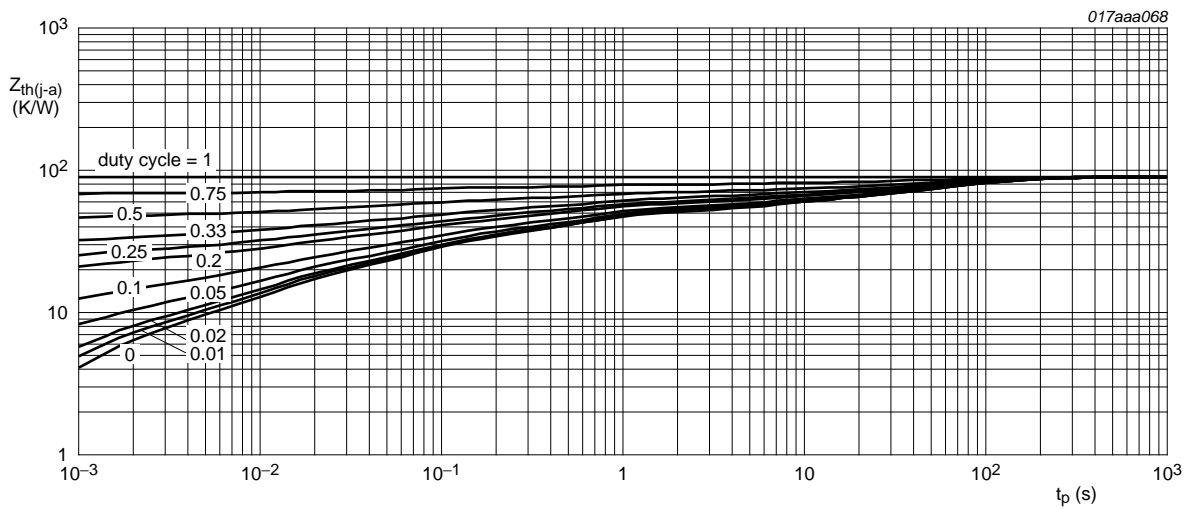
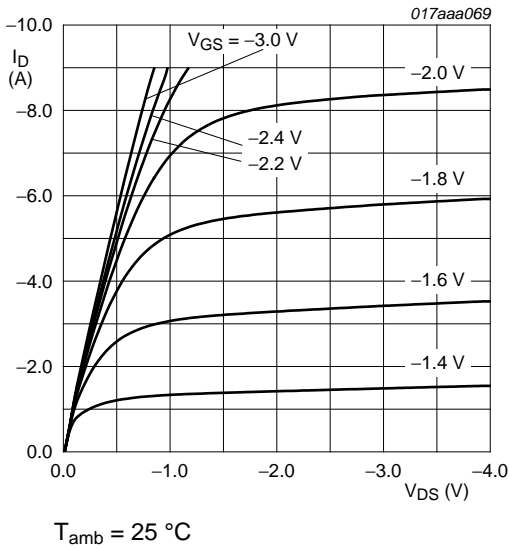


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

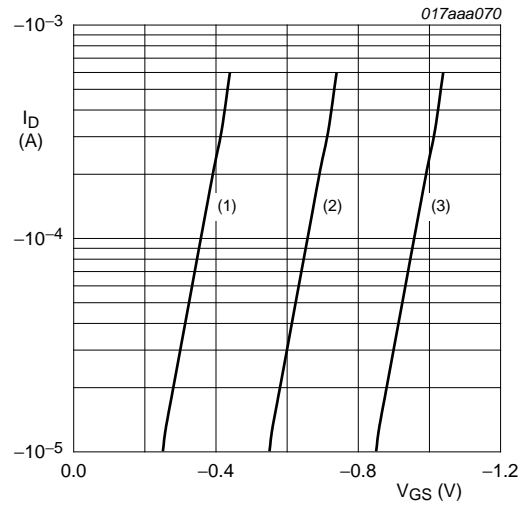
## 7. Characteristics

Table 7. Characteristics

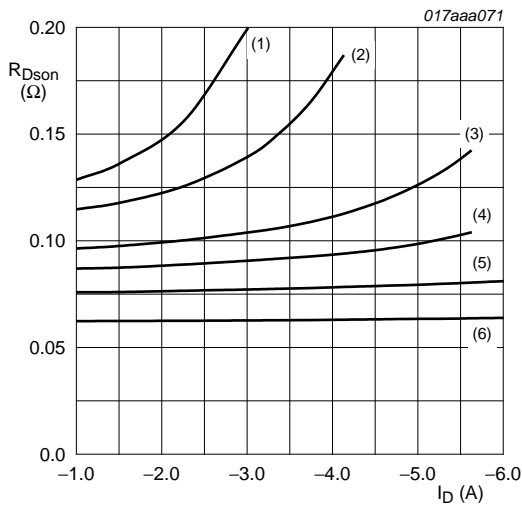
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.4	-0.7	-1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu A$
		$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1	10	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-1	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V$ ; $I_D = -1 A$ ; $t_p \leq 300 \mu s$ ; $\delta \leq 0.01$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	58	70	m $\Omega$
		$V_{GS} = -4.5 V$ ; $I_D = -1 A$ ; pulsed; $t_p \leq 300 \mu s$ ; $\delta \leq 0.01$ ; $T_j = 125 \text{ }^\circ\text{C}$	-	80	100	m $\Omega$
		$V_{GS} = -2.5 V$ ; $I_D = -1 A$ ; $t_p \leq 300 \mu s$ ; $\delta \leq 0.01$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	72	90	m $\Omega$
		$V_{GS} = -1.8 V$ ; $I_D = -0.5 A$ ; $t_p \leq 300 \mu s$ ; $\delta \leq 0.01$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	100	150	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -5 V$ ; $I_D = -1 A$ ; pulsed; $t_p \leq 300 \mu s$ ; $\delta \leq 0.01$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	8	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$I_D = -3.3 A$ ; $V_{DS} = -10 V$ ; $V_{GS} = -4.5 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	6	nC
$Q_{GS}$	gate-source charge		-	0.8	-	nC
$Q_{GD}$	gate-drain charge		-	1	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 V$ ; $V_{DS} = -10 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	380	-	pF
$C_{oss}$	output capacitance		-	72	-	pF
$C_{rss}$	reverse transfer capacitance		-	61	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V$ ; $R_L = 15 \Omega$ ; $V_{GS} = -8 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	5	-	ns
$t_r$	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	57	-	ns
$t_f$	fall time		-	35	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.3 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.75	-1	V



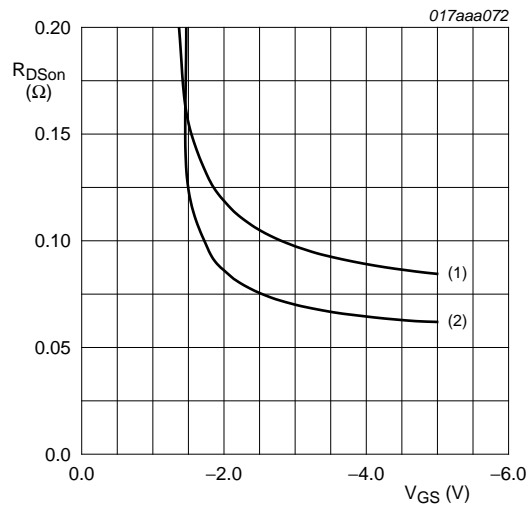
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



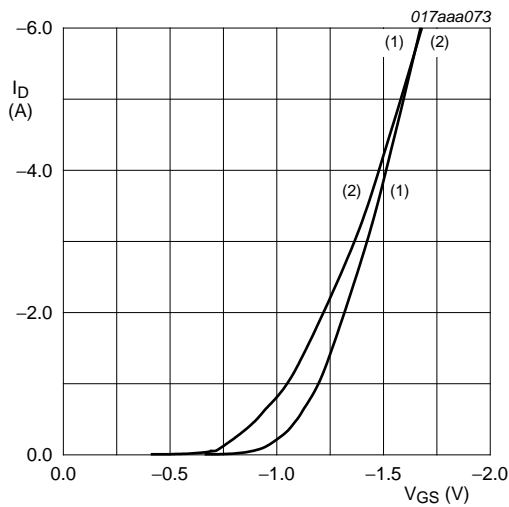
**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**

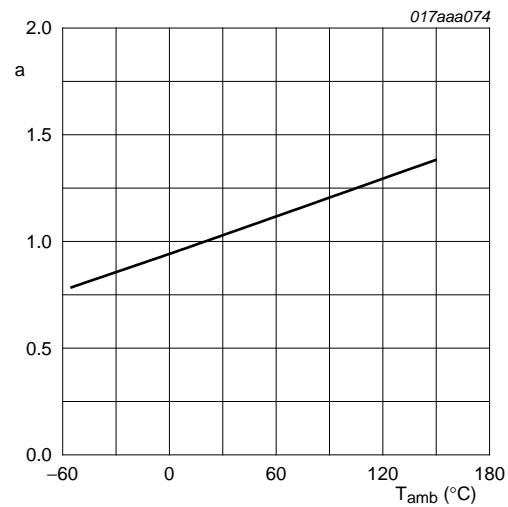


**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



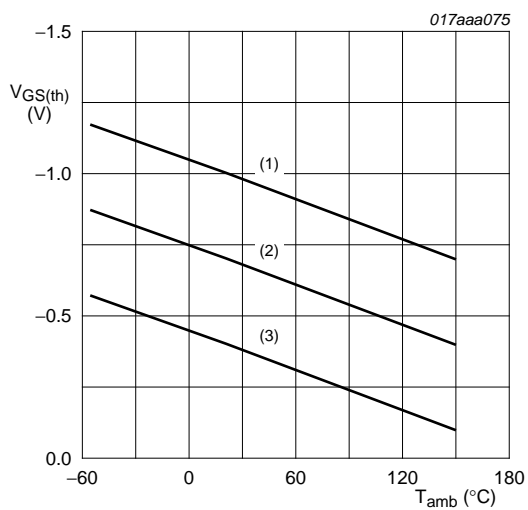
$V_{DS} > I_D \times R_{DSon}$   
 (1)  $T_{amb} = 25\text{ °C}$   
 (2)  $T_{amb} = 150\text{ °C}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



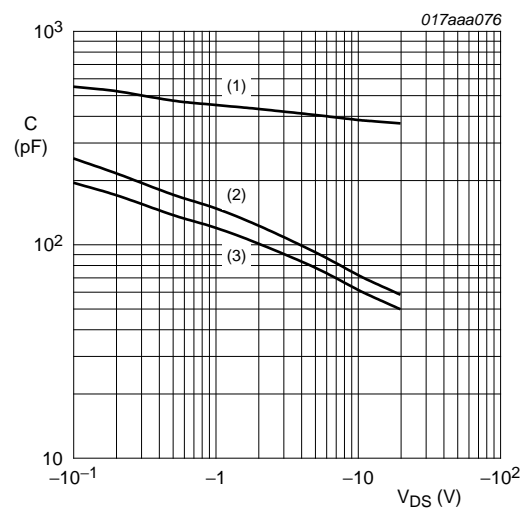
$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values**



$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

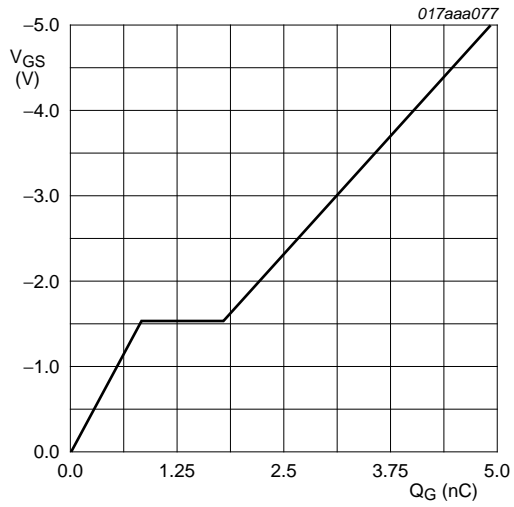
**Fig 12. Gate-source threshold voltage as a function of ambient temperature**



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

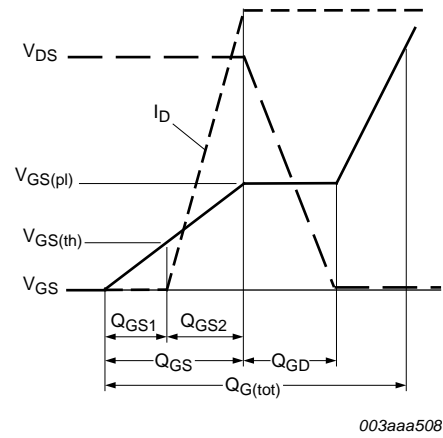
**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





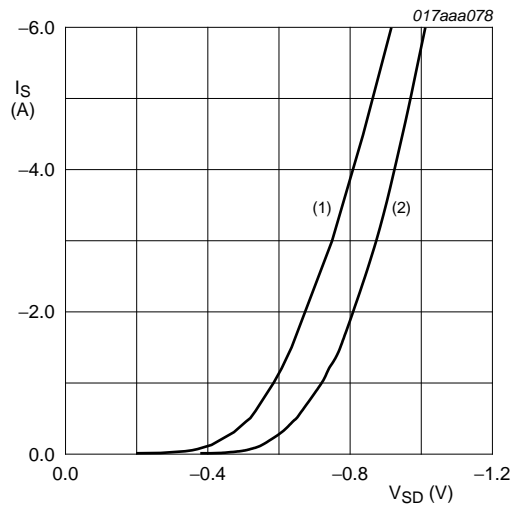
$I_D = -3.3 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



003aaa508

**Fig 15. Gate charge waveform definitions**



$V_{GS} = 0 \text{ V}$   
 (1)  $T_{amb} = 150 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

8. Package outline

HUSON6: plastic, thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1118

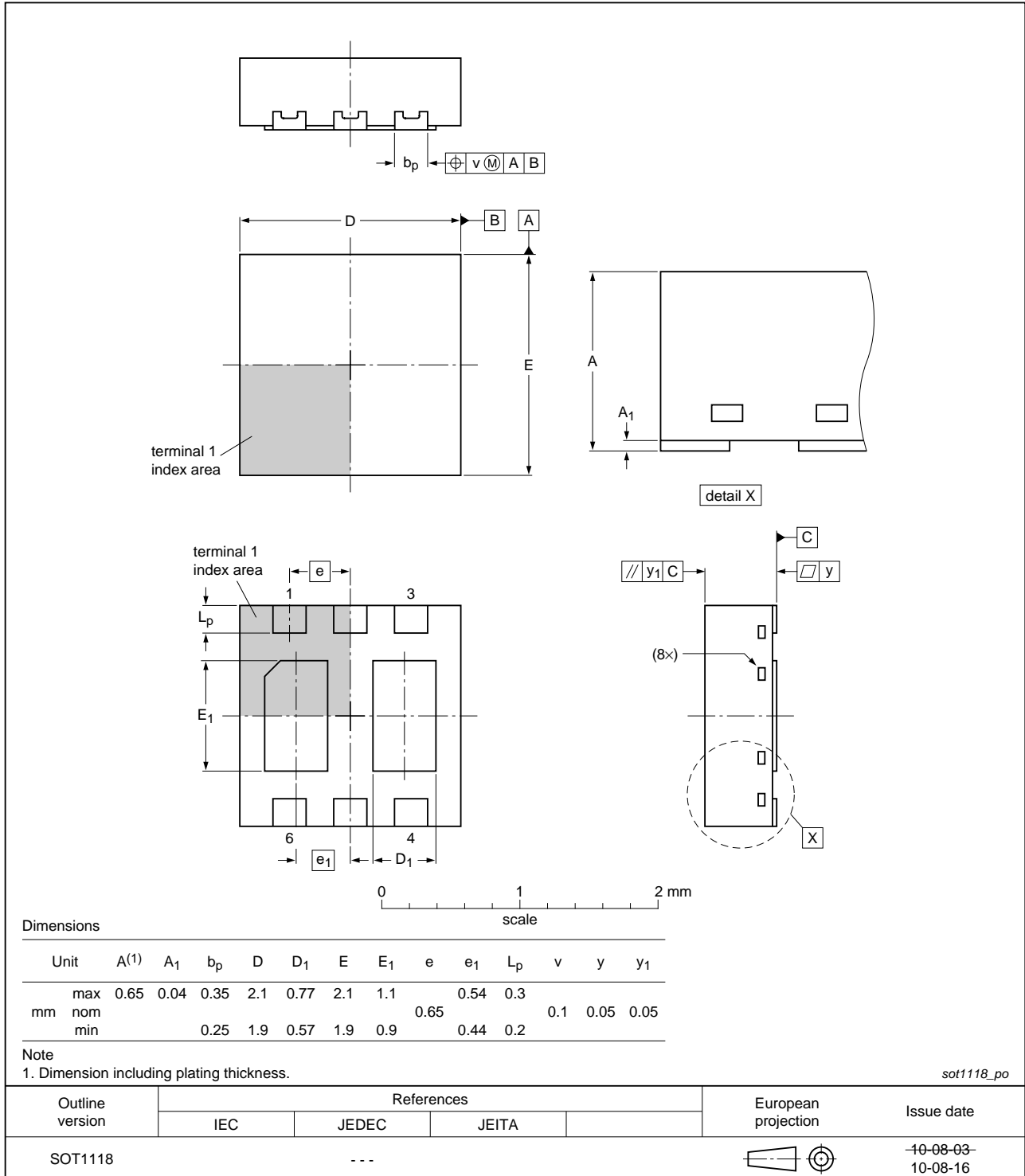
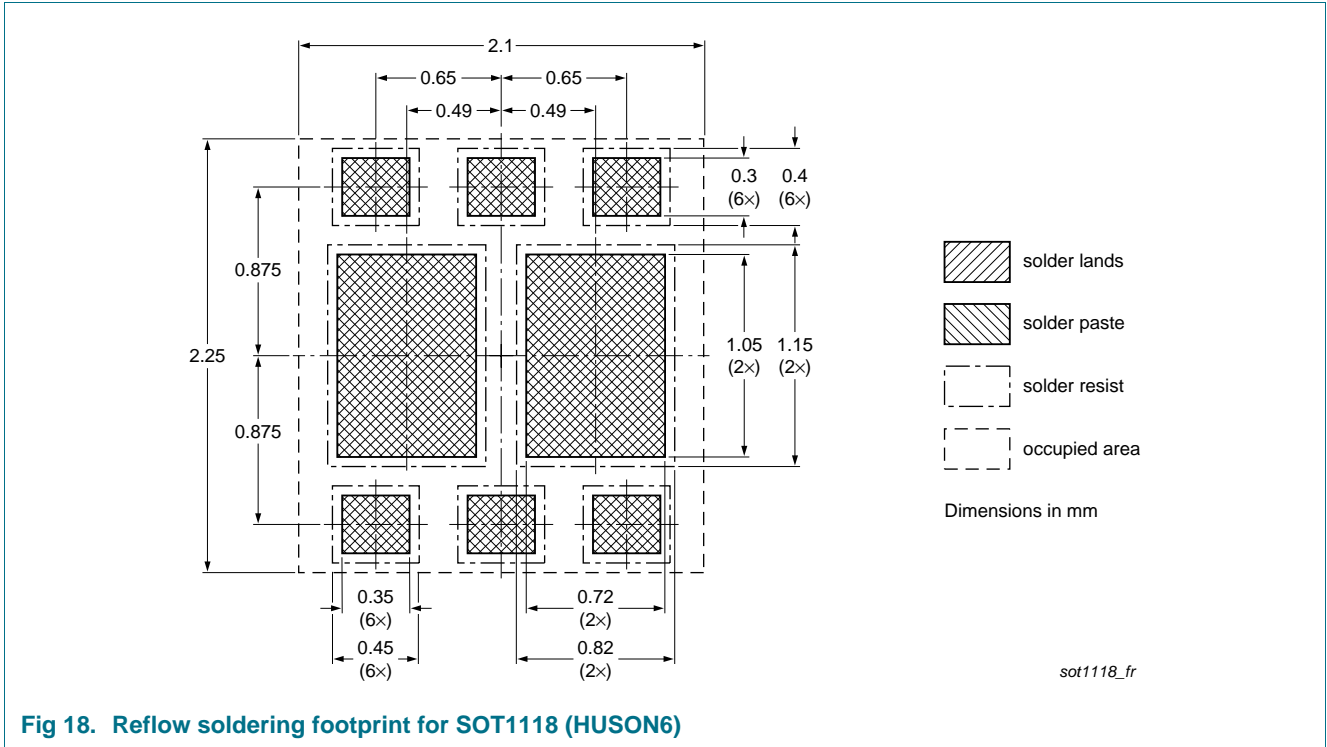


Fig 17. Package outline SOT1118 (HUSON6)

**9. Soldering**



**Fig 18. Reflow soldering footprint for SOT1118 (HUSON6)**

## 10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB65UP v.2	20110308	Product data sheet	-	PMDPB65UP v.1
Modifications:	• <a href="#">2 "Pinning information"</a> : corrected.			
PMDPB65UP v.1	20110118	Product data sheet	-	-

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Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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