MPC8572EAMC Advanced Mezzanine Card User Guide

MPC8572EAMCUG
Rev. 1.2
11/2008

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Document Number: MPC8572EAMCUG
Rev. 1.2, 11/2008

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Chapter 1
General Information

1.1 Introduction

This document describes the MPC8572EAMC AdvancedMC (AMC). The MPC8572EAMC provides an AdvancedMC debugging platform for engineers developing applications for the MPC8572E series of Freescale Processors.

The MPC8572E family of processors is designed to offer clock speeds from 1.2 GHz up to 1.5 GHz, combining two powerful e500 processor cores, enhanced peripherals and high-speed interconnect technology to balance processor performance with I/O system throughput. These processors also include a next-generation double data rate (DDR2/DDR3) memory controller, enhanced Gigabit Ethernet support, double precision floating point and an integrated security engine that features updated advanced encryption standard (AES) functionality.

The MPC8572EAMC single-width AdvancedMC board is designed around the dual-core feature set of the MPC8572E microprocessor. Each integrated 32-bit wide DDR2/3 controller connects to a separate 1-GByte DDR2 SoCDIMM (2 GBytes in total). For control plane applications, two SGMII Ethernet ports are connected to AdvancedMC ports 0 and 1. The other two SGMII Ethernet ports of the MPC8572E are connected to the front panel of the card, as well as an additional 10/100 Fast Ethernet port. A dual USB debug port and board reset switch, are also connected to the front card panel.

128 Mbytes of FLASH memory is available on the AdvancedMC for file/OS storage. AdvancedMC board management is handled via a CorEdge™-enabled module management controller based around a Freescale MCF5213. This provides the board with power sequencing, hot swap functionality, temperature sensing, and FRU record storage.

Finally, high-speed Serial RapidIO™ links are connected from the MPC8572E to AdvancedMC ports 8–11 (and optionally, via resistor links to AdvancedMC ports 4–7). PCI-Express™ connectivity is available on AdvancedMC ports 4–7 (PCI-Express functionality is mutually exclusive with Serial RapidIO functionality on AdvancedMC ports 4–7).

1.2 Working Configuration

There is one configuration for use with the MPC8572EAMC board, which is system development in an AdvancedMC-compatible chassis.

1.2.1 System Development Configuration

The recommended procedure when configuring the MPC8572EAMC is to run the card using an ATCA, MicroTCA, picoTCA or equivalent chassis. This allows the correct power and air flow to be delivered to

the board. AdvancedMC boards must be inserted into carrier chassis as directed by the specific carrier's instructions. As in standard development systems, these chassis provide direct connections to JTAG and external connections.

1.3 MPC8572EAMC Processor Board

In the following subsystems a detailed description of the board and its connectors is provided.

- Target Use
  - System component for media gateway and RNC systems
  - Software development platform for media gateway and RNC systems
  - System design reference/enablement platform for customers and third parties
- Form Factor
  - Single width AdvancedMC size, full height module
- Connectivity
  - 2x1000 Base-X Gigabit Ethernet from backplane AdvancedMC ports 0 and 1 to MPC8572E eTSEC3/4 via SGMII PHY
  - 2x1000 Base-T Gigabit Ethernet from AdvancedMC front panel (dual RJ-45) to MPC8572E eTSEC1/2 via SGMII PHY
  - 1x 10/100 BaseT from AdvancedMC front panel (single RJ-45) directly to MPC8572E FEC via RGMII
  - Dual core serial connectivity on AdvancedMC front panel via mini-Type B USB connector (multiplexed)
  - x4 Serial RapidIO interfaces on backplane AdvancedMC ports 8–11, connected to MPC8572E SerDes block
  - x4 PCI-Express interface on backplane AdvancedMC ports 4–7, connected to MPC8572E SerDes block
  - Option to connect x4 Serial RapidIO on backplane AdvancedMC ports 4–7 (at expense of PCI-Express)
- Hardware Blocks
  - MPC8572E:
    - Two high-performance Power Architecture™ e500v2 cores with 36-bit physical addressing
    - 1024-Kbyte level 2 cache
    - Integrated security engine with XOR acceleration
    - 4 × 1 GEth enhanced 3-speed Ethernet controllers (SGMII-capable)
    - 10/100 Fast Ethernet controller maintenance interface
    - 2x DDR2/DDR3 SDRAM memory controllers, one per core
    - 3x PCI Express controllers
    - 1x Serial RapidIO controller with RapidIO messaging unit
    - 2x UART
    - Local Bus Controller

- GPIO
- IEEE Std 1149.1™ interface

— Board Management
- Hot Swapping
- FRU Storage
- Status LEDs
- Temperature and voltage monitoring

— Power Supply
- 12-V and 3.3-V IPMCV, provided via AdvancedMC edge connector
- On-board voltage requirements are generated via DC-DC voltage regulators:
  - 3.3 V for I/O
  - 1.1 V for CPU core voltage
  - 2.5/1.2 V for Ethernet PHYs
  - 1.8/0.9 V for DDR2 SoCDIMMs

— Configuration
- MPC8572E POR configs controlled via user defined DIP switches: SW5, 500, 501
- Additional User switches provided (x4): SW4
- Front panel user reset switch: SW3
- Master reset switch: SW2
- AdvancedMC ports 4–7 selected via soldered resistor links (option A/B)

— MPC8572E Debug
- Chained JTAG header for Reset/System CPLDs
- 16-pin COP header for processor debug

1.3.1 External Connectors

The MPC8572EAMC interconnects with external devices via the following set of connectors

- Front Panel, Dual Ethernet Connector (for Eth0/1—GigEth) (P3)
- Front Panel, Single Ethernet Connector (for Eth4—FEC) (P1)
- AdvancedMC Edge Connector (P2)
- USB Mini-Type B connector (J2)
- IEEE Std 1588™ Header for Ethernet test (J1)
- USB DUART Connection. Provides debug information from MPC8572E Core #0 /1 (J2).
- MMC BDM Debug header. Reserved for factory use only (J3).
- MPC8572E COP Debug header (J4)
- CPLD JTAG Select. Reserved for factory use only (J6).
- CPLD Programming Header. Reserved for factory use only (HD1).
- MMC Console debug: Pin 1 = TxD, Pin 2 = RxD, Pin 3 = GND (J7)

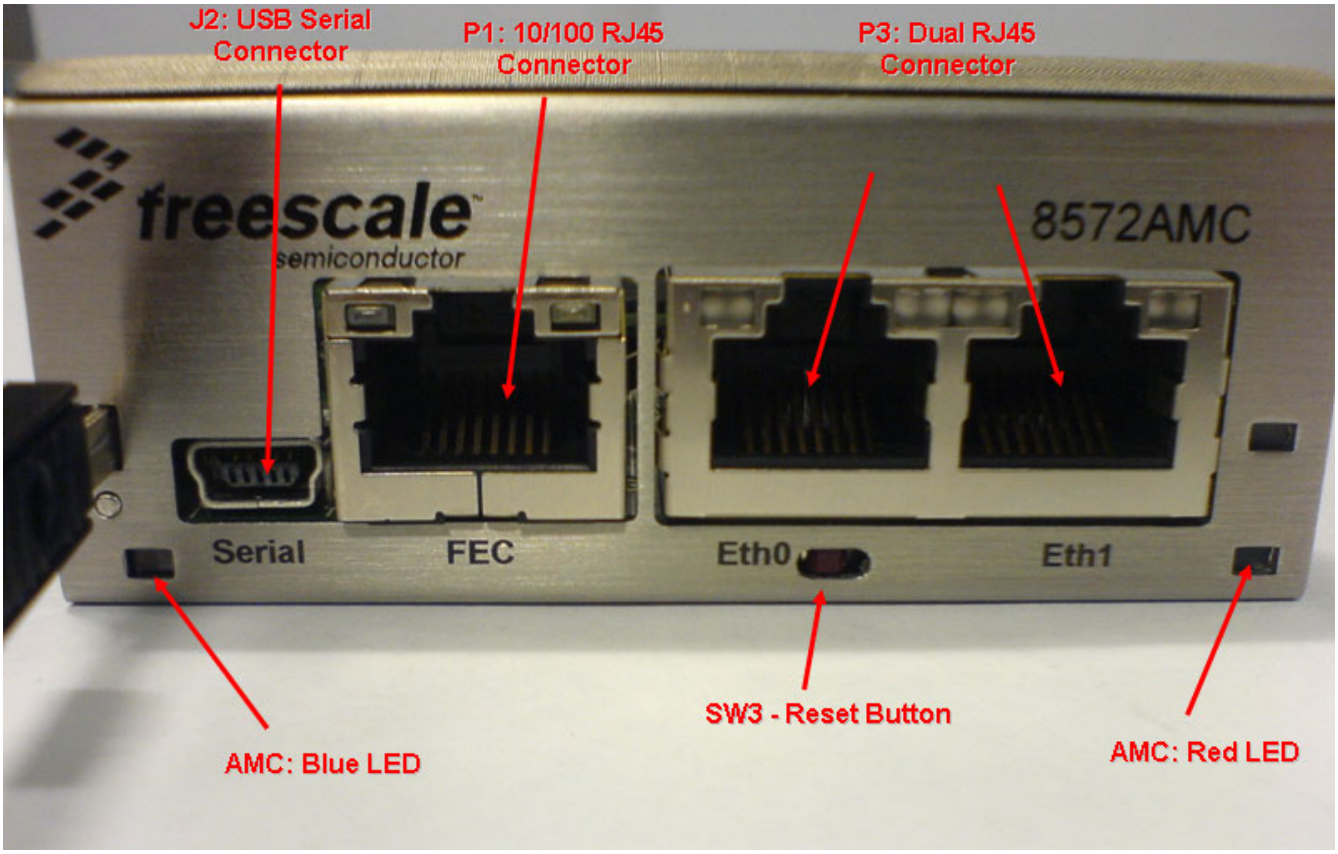

Figure 1-1. MPC8572EAMC Board Front Panel Connections

NOTE

Users should note that the MPC8572EAMC is shipped with the “U-Boot” bootloader and a Linux Kernel already programmed into the FLASH memory. The Linux kernel uses the ETH0–4 notation, whereas eTSEC1–4 and FEC is the notation used by U-boot.

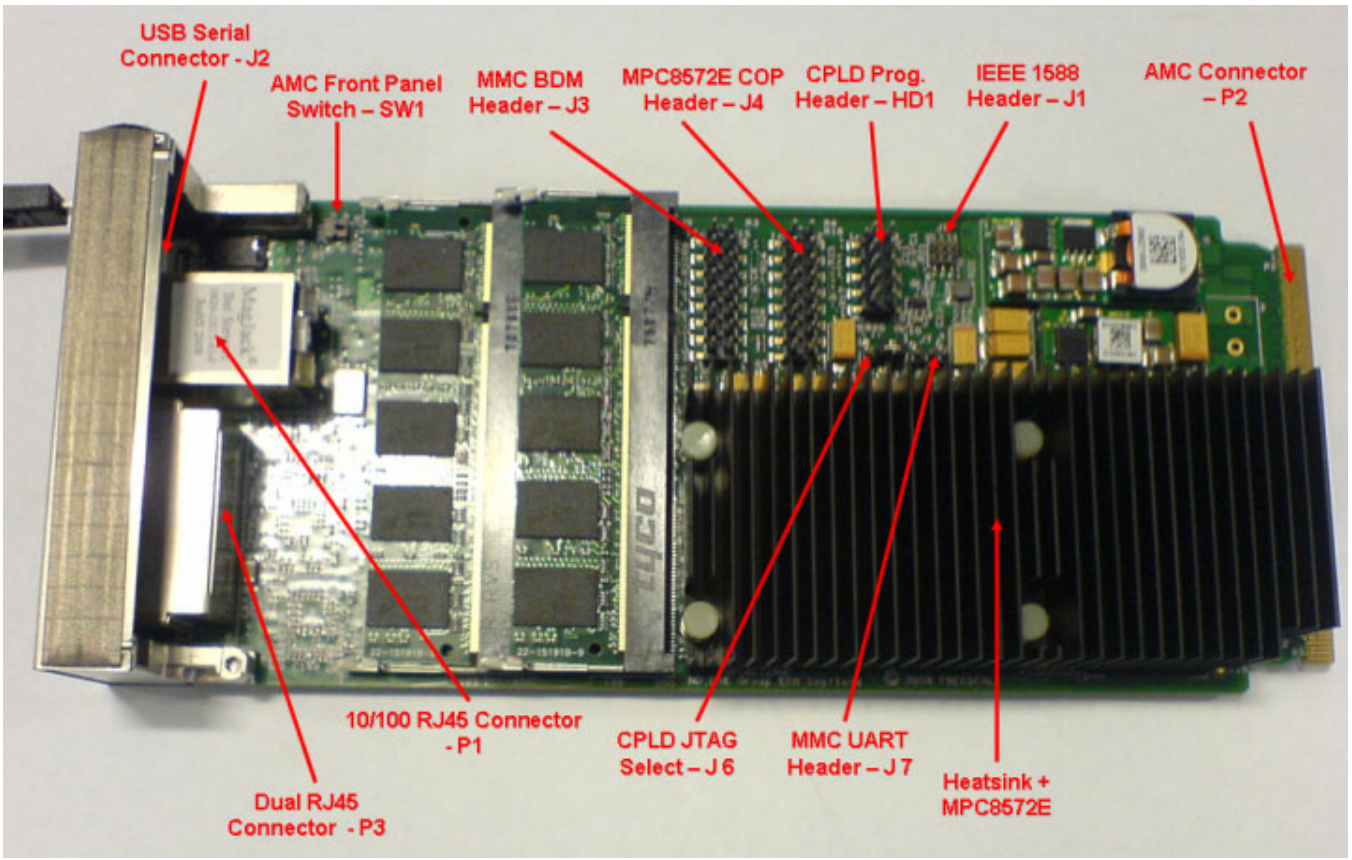

Figure 1-2. MPC8572EAMC Board External Connections

1.4 MPC8572EAMC Block Diagram

Figure 1-3 shows the block diagram for the MPC8572EAMC.

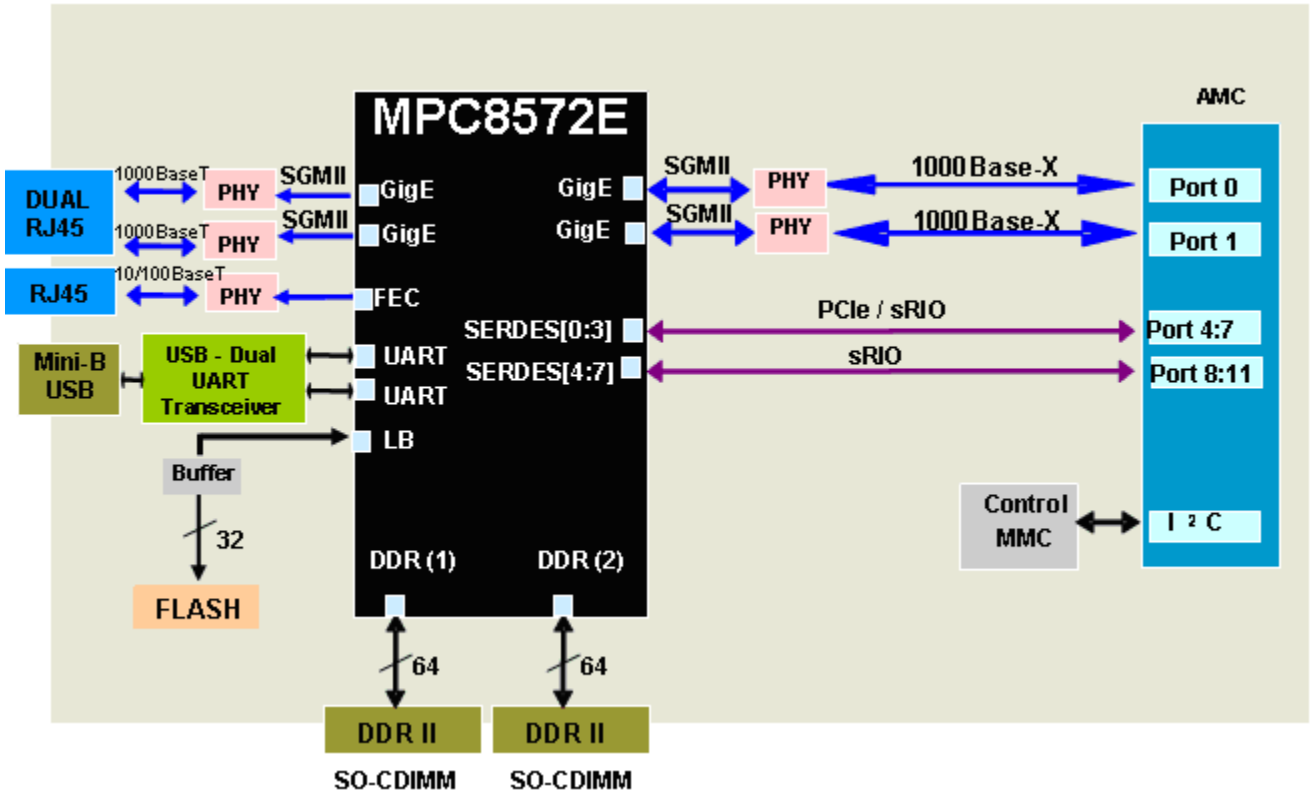

Figure 1-3. MPC8572EAMC Block Diagram

1.5 Definitions, Acronyms, and Abbreviations

Table 1-1 lists definitions, acronyms, and abbreviations.

Table 1-1. Definitions, Acronyms, and Abbreviations

Acronym	Definition
AdvancedMC	Advanced mezzanine card
ATCA	Advanced telecommunications computing platform
BDM	Background debugging mode
CPLD	Complex programmable logic device
DIP	Dual in-line package
DNP	Do not populate
DSP	Digital signal processor
DUART	Dual universal asynchronous receive transmit

Table 1-1. Definitions, Acronyms, and Abbreviations (continued)

Acronym	Definition
EEPROM	Electrically erasable programmable read-only memory
GETH	Gigabit Ethernet
HW	Hardware
I2C (BUS)	Inter-IC bus
MMC	Module management controller
POR	Power-on reset
TLA	Technology license agreement
UART	Universal asynchronous receive transmit
µTCA	Micro telecommunications computing platform

1.6 Related Documentation

This document references the following documents:

- *MPC8572EAMC Hardware Getting Started Guide* (MPC8572EAMCGSG)
- *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* (MPC8572ERM)
- *MPC8572E PowerQUICC™ III Integrated Host Processor Hardware Specification* (MPC8572EEC)
- *PICMG AMC.0 R2.0, Advanced Mezzanine Base Card Specification*
- *PICMG AMC.1, R1.0, AdvancedMC PCI Express and AS*
- *PICMG AMC.2 AdvancedMC Ethernet*
- *PICMG AMC.4 AdvancedMC Serial RapidIO*

1.7 Specifications

Table 1-2 lists the specifications for the AdvancedMC board.

Table 1-2. AdvancedMC Board Specifications

Characteristics	Specifications
Power requirements	No external power supply for AdvancedMC modes—powered from ATCA carrier/uTCA chassis.
Operating temperature	0 C to 70 C
Storage temperature	–25 C to 85 C

Table 1-2. AdvancedMC Board Specifications (continued)

Characteristics	Specifications
Relative humidity	5% to 90% (non condensing)
Dimensions	Single width AdvancedMC form factor Length = 1806. mm Width = 73.5 mm Height = 17.91 mm Board thickness = 1.6 mm

Table 1-3 lists the specifications processing support.

Table 1-3. Processing Support

Subsystem	Component	Specifications
MPC8572E	Processor core/speed	Dual cores running up to 1.5 GHz
Memory	EEPROM	x32 128-Mbyte
	DDRII	2 Gbytes, 32-bit wide DDR2 (up to 800 MHz) (2 × 1 Gbyte SoCDIMMS)
Communication ports	Gigabit Ethernet	SGMII GigE SERDES from MPC8572E to front and back panels.
	Fast Ethernet	RGMII 10/100 Ethernet from MPC8572E to front panel.
	Serial RapidIO	x1/x4 Serial RapidIO Switch configurable for 1.25/2.5 or 3.125 Gbps data rate
	PCI-Express	x4 capability on AdvancedMC ports 4–7 (Option A resistor configuration) 2.5 Gbps.
	UART	RS232-USB transceiver allows data exchange from both cores.

Chapter 2
Hardware Preparation and Installation

This chapter details the unpacking instructions, hardware preparation and installation instructions for the MPC8572EAMC processor board. For details on hardware preparation, please refer to the *MPC8572EAMC Hardware Getting Started Guide* (MPC8572EAMCGSG).

2.1 Unpacking Instructions

NOTE

Upon receipt, if the shipping carton is damaged, request the carrier agent be present during the unpacking and inspection of the equipment.

CAUTION

Avoid touching areas of integrated circuitry as static discharge can damage board devices.

- Unpack equipment from shipping carton
- Refer to packing list and verify that all items are present
- Save packing material for storing and reshipping of equipment

2.2 Installation Instructions

Perform the following steps in the order listed to install the MPC8572EAMC Processor Board properly.

1. Verify that jumpers and switches are in their default positions (See Chapter 4, “Controls and Indicators,” for a list of default positions).
2. Connect external cables in accordance with your needs (See Section 1.3.1, “External Connectors,” for more details).
3. Insert the board into the carrier/chassis as per the specific chassis operating instructions.
4. Switch on the power to the chassis.
5. Check for completion of the reset sequence indicated by the LEDs; see Figure 4-1 for locations. A full description of the LEDs is given in Table 4-3.
6. Check for the blue front panel LED and power good LEDs being illuminated. (A full description of the LED operation is given in Section 4.3, “LEDs”). This indicates the board power is applied.
7. Insert the AdvancedMC front panel handle and check that the blue LED blinks twice then goes out. Then check for completion of the reset sequence by verifying the following LEDs:
   — The “System Status” LED, LD507, switches on, then goes off once system configuration is complete. LD506 should stay on indicating the processor is “Ready.”

8. Ethernet backplane port activity LEDs D501, D502 (for ETH2/eTSEC2-AMC Port 0) and LEDs D504, D505 (for ETH3/eTSEC3-AMC Port 1) are illuminated if there is a physical network link on Port 0 or 1 of the AdvancedMC backplane.
9. Ethernet front panel activity is indicated on the front panel LEDs of the respective RJ-45 PHY connections.
10. USB UART activity is shown on LEDS D507 and D508. A USB cable must be connected between the host PC and the front panel USB connector. A serial terminal can be set up using a PC communication program, such as HyperTerminal, set to 115200-8-N-1 baud rate. If the USB session disconnects (for example, when power is cycled), then the communication link must be disconnected and reconnected again.
11. Pressing the front panel reset button SW3 resets the board and starts the reset sequence.
12. Pressing the reset button SW2 power-cycles the board and starts the reset sequence.
13. Operate the CodeWarrior IDE software to verify that the board is installed properly

Chapter 3
Memory Map

The MPC8572EAMC is shipped with the following memory map as described in Table 3-1.

Table 3-1. MPC8572EAMC Memory Map

Base Address	Device	Size
0x0000_0000	DDR Controller 1 (64-bit)	1 Gbyte
0x4000_0000	DDR Controller 2 (64-bit)	1 Gbyte
0x8000_0000	PCI Express Memory	1 Gbyte
0xC000_0000	Serial RapidIO Controller	512 Mbytes
0xF800_0000	Local Bus FLASH	128 Mbytes
0xFFC0_0000	PCI-Express I/O	64 Kbytes
0xFFE0_0000	CCSR	1 Mbyte

Chapter 4
Controls and Indicators

This chapter describes the controls and indicators for the MPC8572EAMC processor board, which includes switches, jumpers, LEDs, and push button switches, shown in Figure 4-1.

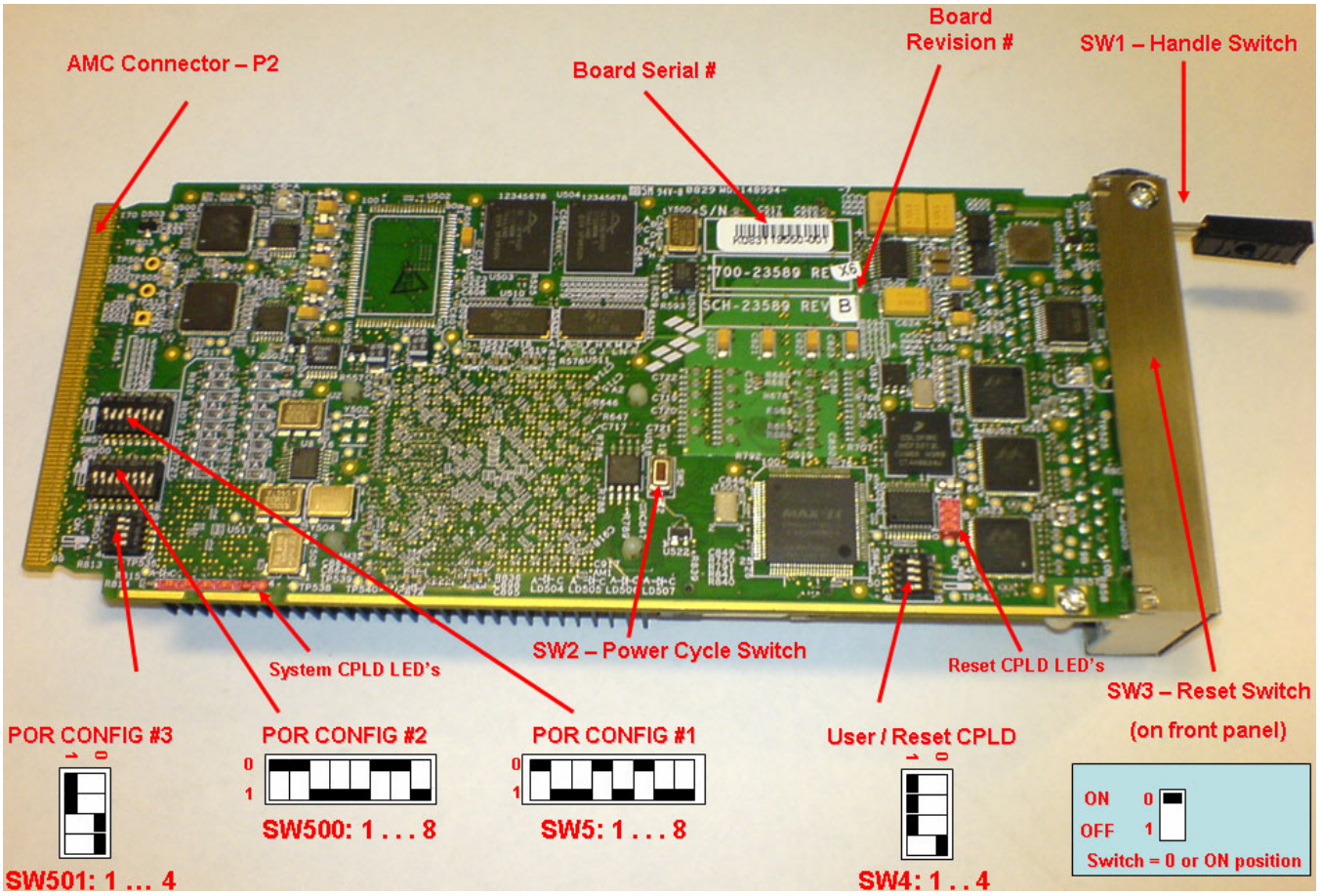

Figure 4-1. MPC8572EAMC—Switches, Jumpers, LEDs and Push Buttons

4.1 DIP Switch Settings

Figure 4-1 shows the location of the DIP switches on the board and their default (factory) position. Table 4-1 describes the possible settings of all DIP switches on the boards. Note that when in the "ON" position, the value of the switch is zero. For a detailed description of the bits and fields, refer to the Section 4.4.3, "Power-On Reset Configuration" in the *MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual, Revision 2.*

Table 4-1. MPC8572EAMC DIP Switch Listing

Feature	Default Settings [OFF = 1, ON = 0)	Comments
SW4		
SW4.1	OFF	Reserved
SW4.2	OFF	Reserved
SW4.3	OFF	Reserved
SW4.4	ON	[SW4.4] = MMC H/W Select. ON—MMC present[1] [SW4.4] = MMC H/W Select. OFF—MMC not present
SW5		
SW5.1	ON	[SW5.1:2] = ON:ON. CCB:SYSCLK = 4:1 (266 MHz) [SW5.1:2] = OFF:ON. CCB:SYSCLK = 8:1 (533 MHz) [SW5.1:2] = ON:OFF. CCB:SYSCLK = 10:1 (666 MHz)[1] [SW5.1:2] = OFF:OFF. CCB:SYSCLK = 12:1 (800 MHz)
SW5.2	OFF	
SW5.3	OFF	[SW5.3:4] = ON:ON. e500 Core #0:CCB = 1.5:1 [SW5.3:4] = OFF:ON. e500 Core #0:CCB = 2:1[1] [SW5.3:4] = ON:OFF. e500 Core #0:CCB = 2.5:1 [SW5.3:4] = OFF:OFF. e500 Core #0:CCB = 3.5:
SW5.4	ON	
SW5.5	OFF	[SW5.5:6] = ON:ON. e500 Core #1:CCB = 1.5:1 [SW5.5:6] = OFF:ON. e500 Core #1:CCB = 2:1[1] [SW5.5:6] = ON:OFF. e500 Core #1:CCB = 2.5:1 [SW5.5:6] = OFF:OFF. e500 Core #1:CCB = 3.5:1
SW5.6	ON	
SW5.7	OFF	[SW5.7:8] = ON:ON. Boot ROM Location = PCI-Express [SW5.7:8] = OFF:ON. Boot ROM Location = Serial RapidIO [SW5.7:8] = ON:OFF. Boot ROM Location = DDR Memory [SW5.7:8] = OFF:OFF. Boot ROM Location = 32-bit Local FLASH Memory[1]
SW5.8	OFF	
SW500		
SW500.1	ON	[SW500.1:3]=ON:ON:ON.DDR Clock Ratio = 3:1 DDRCLK (200 MHz) [SW500.1:3]=OFF:ON:ON.DDR Clock Ratio = 4:1 DDRCLK (266 MHz) [SW500.1:3]=ON:OFF:ON.DDR Clock Ratio = 6:1 DDRCLK (400 MHz) [SW500.1:3]=OFF:OFF:ON.DDR Clock Ratio = 8:1 DDRCLK (533 MHz) [SW500.1:3]=ON:ON:OFF.DDR Clock Ratio = 10:1 DDRCLK (666 MHz)[1] [SW500.1:3]=OFF:ON:OFF.DDR Clock Ratio = 12:1 DDRCLK (800 MHz) [SW500.1:3]=ON:OFF:OFF. RESERVED [SW500.1:3]=OFF:OFF:OFF.DDR Clock Ratio = SYNCHRONOUS
SW500.2	ON	
SW500.3	OFF	

Table 4-1. MPC8572EAMC DIP Switch Listing (continued)

Feature	Default Settings [OFF = 1, ON = 0)	Comments
SW500.4	OFF	[SW500.4:5] = ON:ON. MPC8572E acts as agent on all interfaces [SW500.4:5] = OFF:ON. MPC8572E acts as end point on PCIE #1 host [SW500.4:5] = ON:OFF. MPC8572E acts as end point on SRIO & PCIE #1 host [SW500.4:5] = OFF:OFF. MPC8572E acts as the host processor[1]
SW500.5	OFF	
SW500.6	ON	[SW500.6:8] = OFF:ON:ON. IO Port Selection = SRIO 100-MHz clock, 2.5 Gbps (x4) [SW500.6:8] = ON:OFF:ON. IO Port Selection = SRIO/PCIE 100-MHz clock, 2.5 Gbps [SW500.6:8] = OFF:OFF:ON. IO Port Selection = SRIO/PCIE 100-MHz clock, 1.25/2.5 Gbps (x4) [SW500.6:8] = OFF:ON:OFF. IO Port Selection = SRIO 100-MHz clock, 1.25 Gbps (x4) [SW500.6:8] = ON:ON:OFF. IO Port Selection = SRIO 125 MHz, 3.125 Gbps (x4)[1]
SW500.7	ON	
SW500.8	OFF	
SW501		
SW501.1	OFF	[SW501.1] = ON Boot Sequence Configuration = Boot Sequencer Enabled [SW501.1] = OFF Boot Sequence Configuration = Boot Sequencer Disabled[1]
SW501.2	OFF	CPU Boot Config: [SW501.2:3] = ON:ON.CPU boot hold-off both cores [SW501.2:3] = OFF:ON. E500 Core 0 allowed to boot, Core 1 in boot hold-off[1] [SW501.2:3] = ON:OFF. E500 Core 1 allowed to boot, Core 0 in boot hold-off [SW501.2:3] = OFF:OFF. Both cores boot without external master
SW501.3	ON	
SW501.4	ON	RIO System Size: [SW501.4] = ON. Large system size, up to 65,536 devices[1] [SW501.4] = OFF. Small system size, up to 256 devices

Note:

[1] Default

Check the default positions of the board first and ensure that the board is operational before changing any settings. Please also ensure that the selected settings are within the maximum supported operating characteristics of the device.

4.2 Jumpers

There is one jumper on the board as described in Table 4-2. This jumper is used to include or isolate the System CPLD from the JTAG chain.

Table 4-2. Jumper Position

Jumper	Description
J12	Selects the Reset and System CPLD JTAG chain. • Position 1-2: only Reset CPLD is in the chain • Position 2-3: both Reset and System CPLDs are in the chain.

Note: If the Reset CPLD is blank, then position 1-2 must be used to program it.

4.3 LEDs

Table 4-3 describes the functions of the LEDs on the MPC8572EAMC Processor Board. The physical locations of the LEDs are shown in Figure 4-1.

Table 4-3. LED Description

Description	Ref	Color	LED On	LED Off
MMC red LED	LD1	Red	MMC control	Normal operation
MMC card power blue LED	LD500	Blue	Hot swap state	Hot swap state
Port 0 AMC SERDES Ethernet Rx activity	D500	Green	Rx Ethernet activity	No Rx Ethernet activity
Port 0 AMC SERDES Ethernet Tx activity	D501	Yellow	Tx Ethernet activity	No Tx Ethernet activity
Port 0 AMC SERDES LOS	D502	Orange	Loss of signal	No loss of signal
Port 1 AMC SERDES LOS	D504	Orange	Loss of signal	No loss of signal
Port 1 AMC SERDES Ethernet Tx activity	D505	Yellow	Tx Ethernet activity	No Tx Ethernet activity
Port 1 AMC SERDES Ethernet Rx activity	D506	Green	Rx Ethernet activity	No Rx Ethernet activity
USB/UART 1 activity	D507	Orange	UART 1 activity	No UART 1 activity
USB/UART 0 activity	D508	Orange	UART 0 activity	No UART 0 activity
Front panel dual RJ45 Ethernet Rx activity	P3:D1-2a	Green	Rx Ethernet activity	No Rx Ethernet activity
Front panel dual RJ45 Ethernet Tx activity	P3:D1-4a	Yellow	Tx Ethernet activity	No Tx Ethernet activity
Front panel dual RJ45 Ethernet Rx activity	P3:D1-2b	Green	Rx Ethernet activity	No Rx Ethernet activity
Front panel dual RJ45 Ethernet Tx activity	P3:D1-4b	Yellow	Tx Ethernet activity	No Tx Ethernet activity
Front panel 10/100 RJ45 Ethernet Rx activity	P1	Orange/ Green	Rx Ethernet activity	No Rx Ethernet activity
Front panel 10/100 RJ45 Ethernet Tx activity	P1	Yellow	Tx Ethernet activity	No Tx Ethernet activity
General debug System CPLD	LD507	Green	System CPLD execution not complete	System CPLD execution complete
General debug System CPLD	LD506	Green	Ready signal	POR config cycles unsuccessful
General debug System CPLD	LD505	Yellow	Default on	User debug #1
General debug System CPLD	LD504	Yellow	Default on	User debug #2
General debug POR CPLD	LD502	Green	User config #1	User config #1
General debug POR CPLD	LD501	Yellow	User config #2	User config #2
General debug POR CPLD	LD503	Yellow	User config #3	User config #3

4.4 Headers

The MPC8572EAMC Processor Board has a number of headers used to connect a serial terminal to the module management controller. An additional IEEE 1588 test interface header is also provided. These are detailed in Table 4-4.

Table 4-4. Header Descriptions

Header	Description
J2	MMC serial interface header • Pin1: Serial transmit data output (TxD) • Pin2: Serial transmit data output (RxD) • Pin3: Digital ground (GND)
J10	IEEE 1588 test interface header • Pin1: IEEE 1588 trigger output (trig_out) • Pin2: IEEE 1588 trigger input (trig_in) • Pin3: IEEE 1588 trigger output (pulse_out1) • Pin4: IEEE 1588 trigger output (pulse_out2) • Pin5: IEEE 1588 clock output (clk_out) • Pin6: Spare pull-down resistor

4.5 Push Buttons

Figure 4-2 describes the MPC8572EAMC Processor Board push buttons.

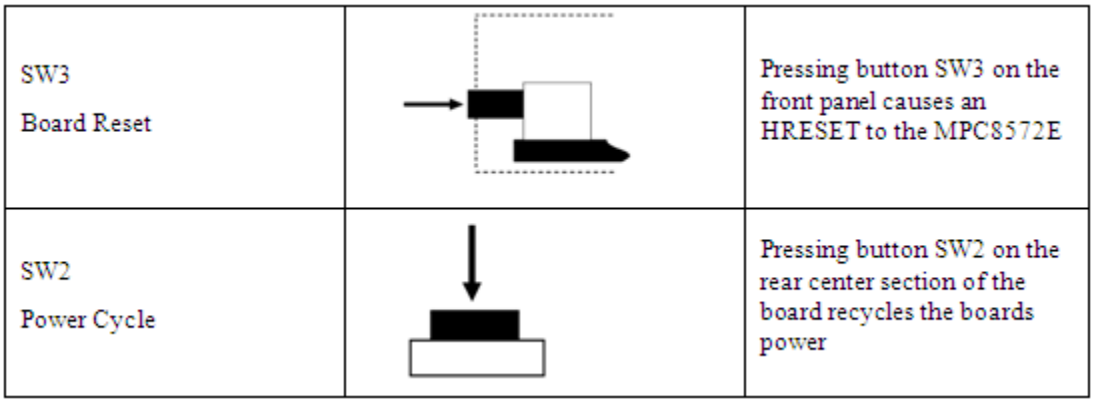

Figure 4-2. MPC8572EAMC Push Button Switches

Chapter 5
MPC8572EAMC Functional Description

This chapter describes the design details of the various MPC8572EAMC hardware blocks. The hardware description has been partitioned into the following logical sections:

- MPC8572E Microprocessor Block
- MPC8572EAMC Ethernet Connectivity
- MPC8572EAMC System Clocking
- MPC8572EAMC Board Control (Power, Reset, Logic)
- AdvancedMC Backplane Connector
- Module Management Controller (MMC)
- Thermal Requirements

The MPC8572EAMC with AMC.1 (PCI Express (and PCI Express Advanced Switching)), AMC.2 (Gigabit Ethernet and XAUI) and AMC.4 (Serial RapidIO interface), fitting into a single-width, full height AdvancedMC. The card contains a single MPC8572E Dual core processor with dual DDR2 memory SoCDIMMs. The MPC8572E has four (SGMII) capable Gigabit Ethernet interfaces, two of which are connected to the backplane via two SGMII PHYs. The other two Gigabit Ethernet interfaces are connected to the front panel onto a dual RJ-45 connector, via two further SGMII PHYs. A further 10/100 Fast Ethernet interface is supported by the MPC8572E and this is connected to the front panel via a RGMII PHY. Serial RapidIO and PCI-Express connectivity to the AdvancedMC backplane is made using high speed SERDES links. Serial (debug) communication with the MPC8572E is made using a mini-type B USB front panel socket that connects to a dual UART-USB transceiver chip. On the local bus of the MPC8572E is located a 128-Mbyte FLASH memory, which is used to store the operating and file systems for the MPC8572EAMC. This FLASH can be programmed directly using debugging tools, such as CodeWarrior, through the MPC8572E microprocessor.

5.1 MPC8572E Microprocessor Block

The MPC8572E microprocessor block consists of a dual core, e500 MPC8572E, dual DDR2/3 memory controllers and associated interfaces.

5.1.1 MPC8572E DDR Memory

The MPC8572E microprocessor provides two 64-bit data DDRII/III interfaces (with 8-bit ECC) up to a maximum data rate of 800 MHz (each core has its own dedicated DDR memory interface). On the MPC8572EAMC there are two Vertium SoCDIMM DIMMs. The VL491T2863T is a 128-Mbit × 72

DDR2 SDRAM high density SO-CDIMM. Control of each memory DIMM is via the MPC8572E's DDR controllers chip select (CS) signals, shown in Table 5-1.

Table 5-1. MPC8572E DDR Chip Select Resources and Memory map

Pin Name	CS Resources	Address	Comments
D1_MCS0	DDR SDRAM	0x00000000	64-bit, controlled by DDR controller #1
D1_MCS1	DDR SDRAM	0x00000000	64-bit, controlled by DDR controller #1
D1_MCS2-3	Unused	Unused	Unused
D2_MCS0	DDR SDRAM	0x40000000	64-bit, controlled by DDR controller #2
D2_MCS1	DDR SDRAM	0x40000000	64-bit, controlled by DDR controller #2
D2_MCS2-3	Unused	Unused	Unused

Figure 5-1 illustrates how the DDR controller interfaces on the MPC8572E device and provides a glueless connection to the two 128-Mbit × 72 SoCDIMMs on the MPC8572EAMC.

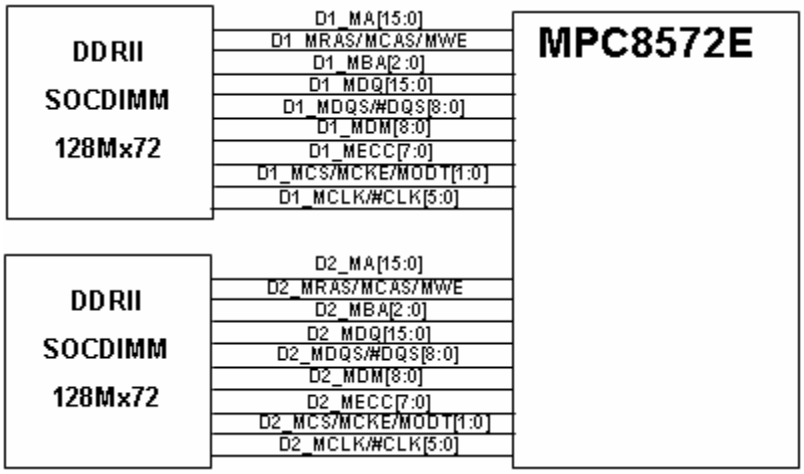

Figure 5-1. DDR2 Connectivity

5.1.1.1 DDR Groups

Every DDR2 signal can be considered to be a member of one of four separate DDR signal groups. Each group has a unique set of rules in terms of their connection and routing on the AdvancedMC board. These four groups are shown in Table 5-2.

Table 5-2. DDR2 Interface Signals

Signal Group	Signal	Description	I/O (w.r.t. Processor)
Address and command	MA[0:15]	Address bus	O
	MBA[0:2]	Bank address bus	O
	#MWE	Write enable	O
	#MCAS	Column address strobe	O
	#MRAS	Row address strobe	O
Control	MCKE[0:3]	Clock enable	O
	#MCS[0:3]	Chip select	O
	MODT[0:3]	On-die termination	O
	MDIC[0:1]	DDR internal calibration	I
Data	MDQS[0:8]	Data strobes	I/O
	#MDQS[0:8]A	Data strobes complement	I/O
	MDM[0:8]	Data mask	O
	MDQ[0:63]	Data bus	I/O
	MECC[0:7]	Error correction bits	I/O
Clocks	MCK[0:5]	Clock	O
	#MCK[0:5]	Clocks complement	O

Complex DDR2 timing adaptation is available via the DDR clocking subsystem of the MPC8572E. It supports the following:

- Sampling of the input data from the DDR2 memory
- Positioning of the DQS output signals during writes to the DDR2 memory
- Synchronizing the incoming DDR2 data to the internal clock
- Control the relationship between output data and CLK_OUT

5.1.1.2 Terminations and I/O Voltage

The DDR2 interface operates at 1.8 V I/O voltages. Reference voltages of 0.9 V are synthesized from a 5-V supply via the TPS51116 voltage regulator. This reference voltage is applied to each DDR2 device (at the VREF pin) and the MPC8572E (at pin MVREF).

The DDR2 interface on the MPC8572E has the addition of the On-Die Termination (ODT) signals. ODT signals are used to control the termination of the data group signals in the DDRII DRAM device. DDR2

uses a termination scheme where the signals terminated in the DRAM device and the controller by internal termination resistors, such as ODT. A compensation capacitor is also not required for the control signals on the board.

5.1.2 Serial RapidIO Interface

The RapidIO controller supports a high-performance, point-to-point, low pin count packet, switched-level interconnect that can be used in a variety of applications as an open standard. The MPC8572E serial RapidIO subsystem complies with the RapidIO Interconnect Specification Revision 1.2, which connects directly to the AdvancedMC backplane. Serial RapidIO is statically connected to AdvancedMC ports 8–11 on the backplane and optionally on AdvancedMC ports 4–7 (which it shares with PCI-Express).

Using serial RapidIO on AdvancedMC ports 4–7 involves desoldering configuration resistors R729, R730, R625, R735, R611, R612, R623, R624, R613, R728, R736, R737, R614, R615, R621 and R622, from the default Option A position (PCI-Express on AdvancedMC ports 4–7) to Option B position (serial RapidIO on AdvancedMC ports 4–7). Figure 5-2 shows the position of these resistors on the MPC8572EAMC board.

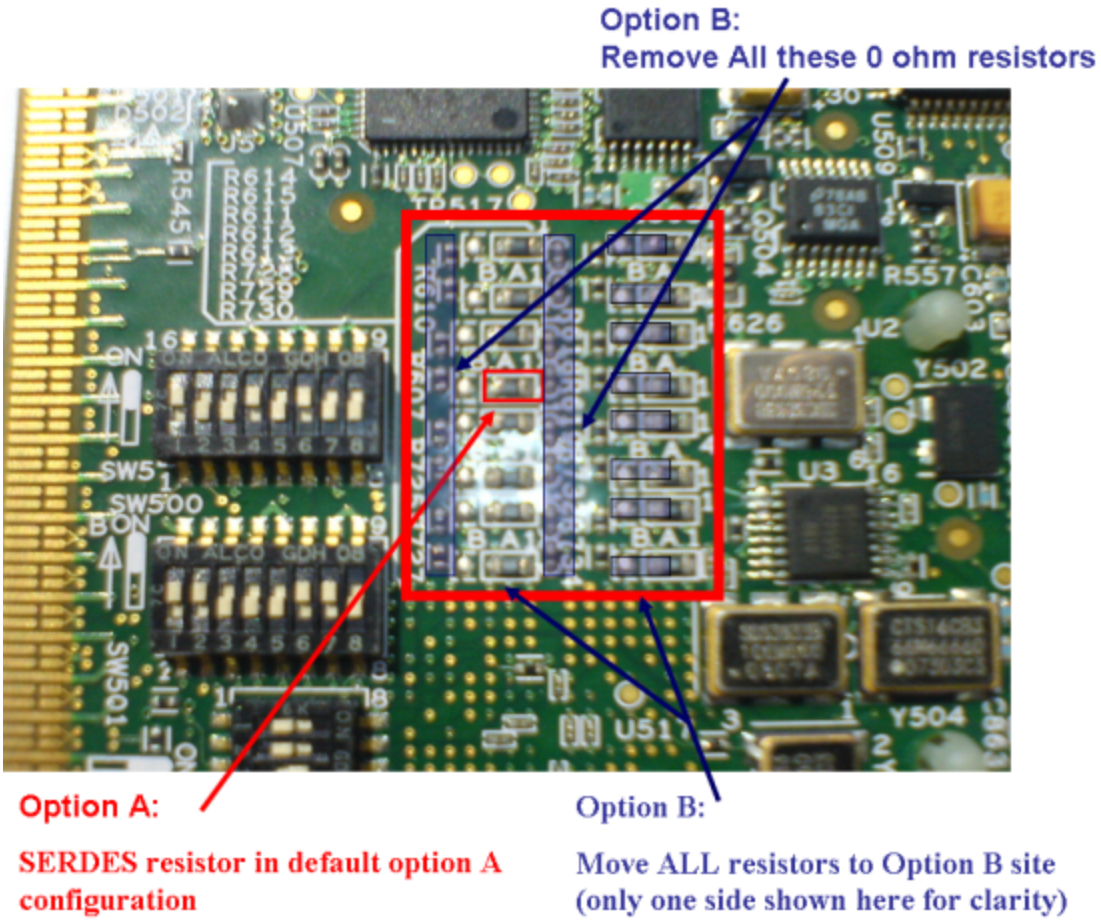

Figure 5-2. Setting SERDES Option A/B

The interface can work in x1 or x4 mode and is selectable via user DIP switches during the POR configuration phase. Table 5-3 illustrates the possible peripheral combinations that are possible on the MPC8572EAMC's fabric port region.

Table 5-3. Serial RapidIO/PCI-Express Board Options

MPC8572EAMC Port #	Option A	Option B
4	PCI-Express x4	SRIO x4
5		
6		
7		
8	SRIO x4	SRIO x4
9		
10		
11		

Figure 5-3 illustrates how the SRIO interface signals are connected to the MPC8572E microprocessor and the AdvancedMC edge connector, and how they relate to the SERDES resistor options.

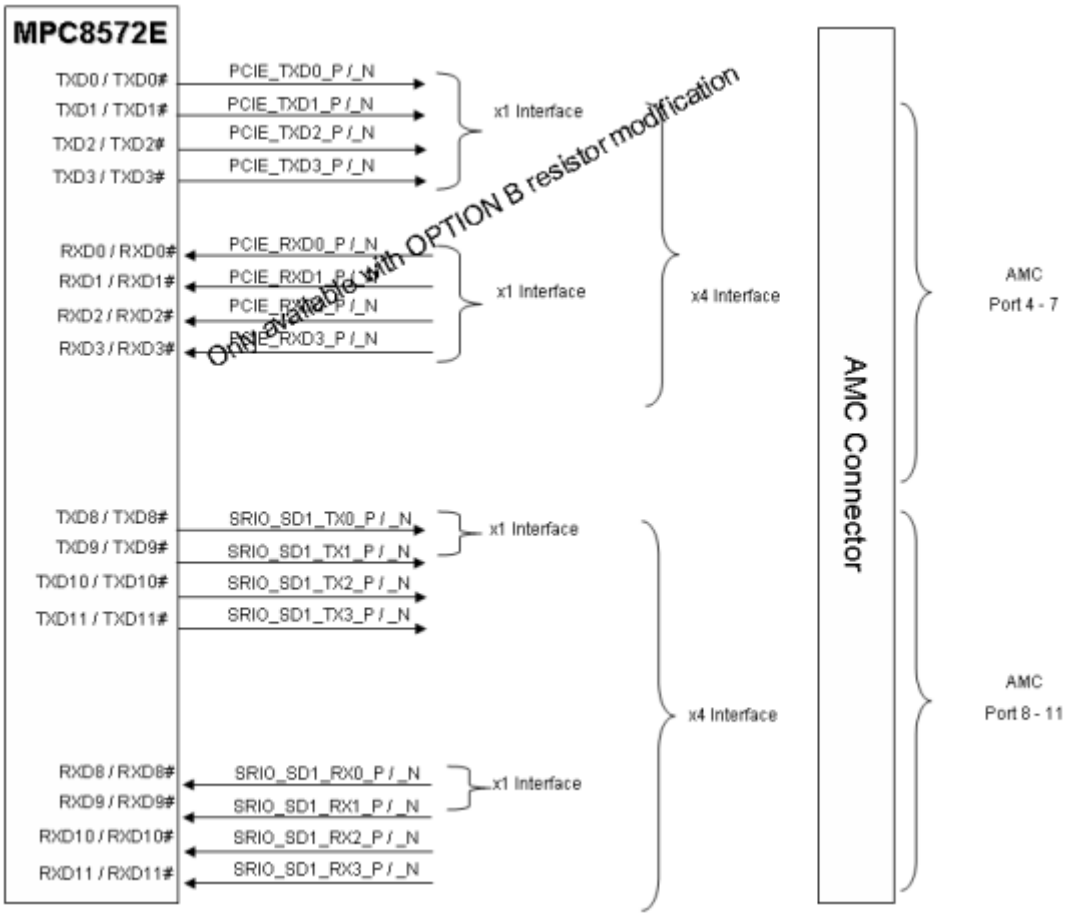

Figure 5-3. Serial RapidIO Connectivity

NOTE

In order for serial RapidIO to co-exist with PCI-Express functionality on the MPC8572EAMC, two SERDES clock rates must be supported: 100 MHz for PCI-Express and 1.25/2.5 Gbps Serial RapidIO, and 125 MHz for 3.125 Gbps Serial RapidIO. Depending on the POR configuration setting for IO configuration bits, this clock frequency is automatically selected by the System CPLD logic.

5.1.3 PCI-Express Interface

The MPC8572E PCI Express interface complies with the *PCI Express™ Base Specification, Revision 1.0a* (available from http://www.pcisig.org). The PCI Express controller connects the internal platform to a 2.5-GHz serial interface. As both an initiator and a target device, the PCI Express interface is capable of high-bandwidth data transfer and is designed to support next generation I/O devices. The PCI Express controller can be configured to operate as either a PCI Express root complex (RC) or an endpoint (EP)

device. An RC device connects the host CPU/memory subsystem to I/O devices while an EP device typically denotes a peripheral or I/O device.

Due to pin multiplexing on the MPC8572E device and the available ports on the AdvancedMC connector, PCI-Express x8 mode does not allow simultaneous use of the Serial RapidIO connection. This is caused by the fact that in x8 mode, PCI-Express uses Port 8–11 onto which the Serial RapidIO is connected. Therefore, x8 PCI-Express is not a supported option. See Table 5-2 for the allowed PCI-Express/Serial RapidIO connections. Figure 5-4 illustrates how the PCI-Express is connected to the MPC8572E microprocessor and the AdvancedMC edge connector.

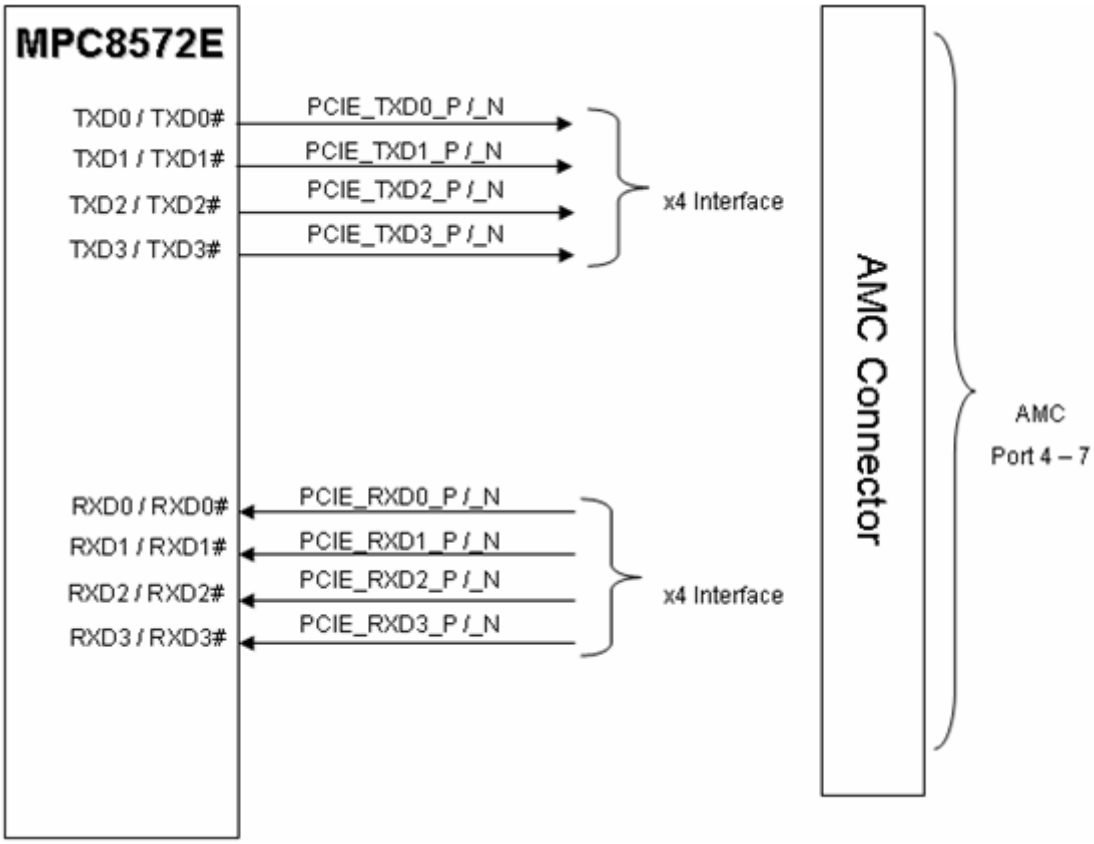

Figure 5-4. PCI-Express Connectivity

5.1.4 Local Bus Interface

The MPC8572E enhanced local bus controller (eLBC) supports three interface types, general purpose chip select machine (GPCM), NAND Flash control machine (FCM) and user programmable machines (UPMs). The LBC memory controller supports up to 8 banks of memory selected via separate different Chip Select signals, these are shown in Table 5-4.

Table 5-4. MPC8572E Local Bus Chip Select Resources and Memory Map

Pin Name	CS Resources	Address	Comments
LCS0	Boot Flash	0xF8000000	32-bit NOR 128-Mbit Flash controlled by GPCM on local bus
LCS1–7	Unused	Unused	Unused

On the MPC8572EAMC, the MPC8572E's 32-bit local bus is used to connect to 128 Mbytes of FLASH memory. This is physically implemented using two AMD S29GL512N Flash devices. In order to minimize the pin count on the MPC8572E device, both the address and data pins are multiplexed. Two SN74ALVCH32973 devices are used on the MPC8572EAMC to both buffer and de-multiplex the MPC8572E local address/data bus signals onto a dedicated address bus and dedicated 32-bit data bus.

Figure 5-5 illustrates how the FLASH ROM is connected to the local bus on the MPC572EAMC.

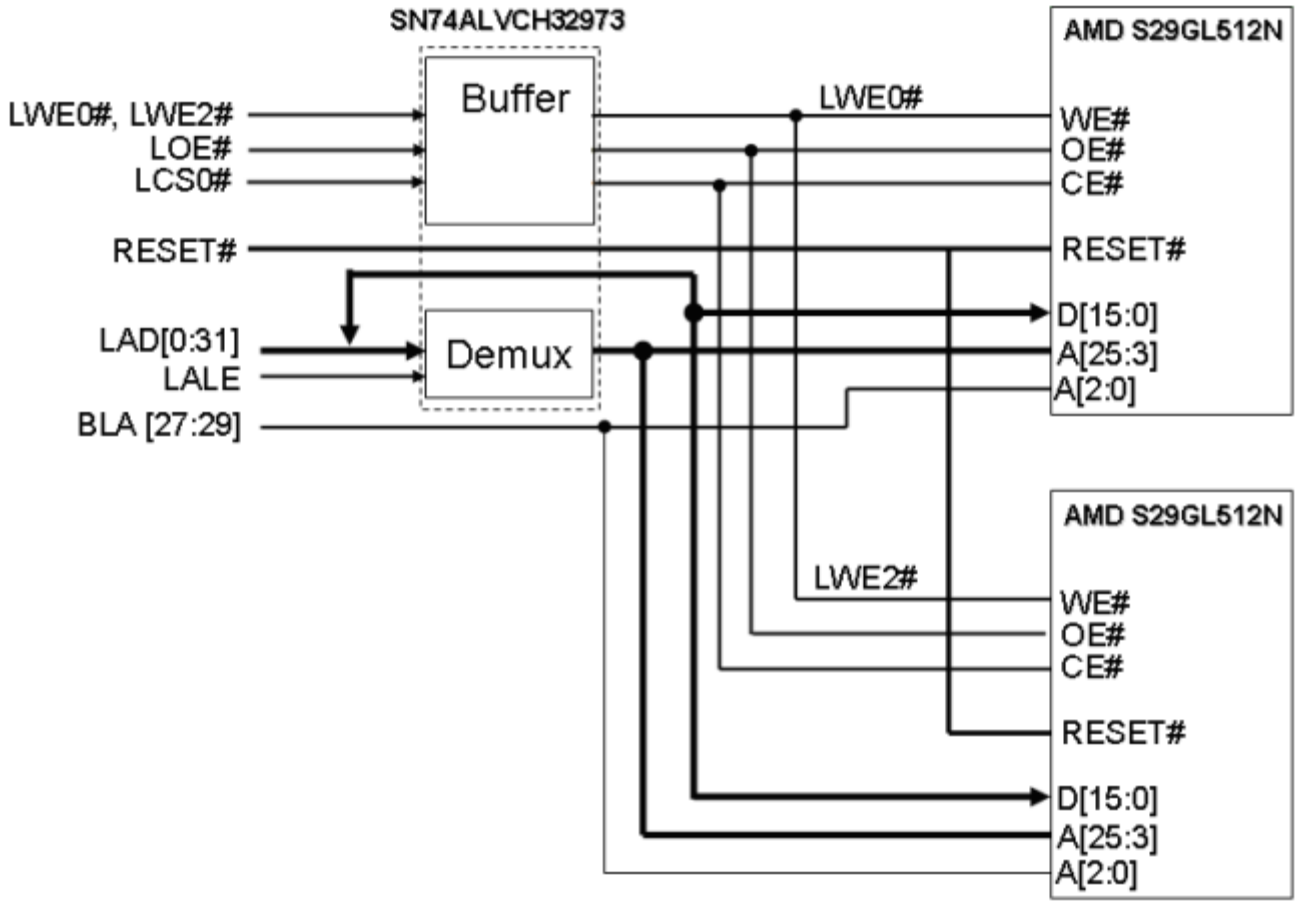

Figure 5-5. Local Bus FLASH ROM Configuration

5.1.4.1 MPC8572E Interrupts

The MPC8572E has a programmable interrupt controller (PIC) unit that prioritizes and manages interrupts from on chip peripherals as well as interrupt signals from three sources: external to the integrated device, internal to the integrated device, and intrinsic to the PIC itself. The PIC has twelve interrupt request lines INT[0–11]. The polarity and sense of each of these signals is programmable, with each being capable of being driven completely asynchronously. Table 5-5 details the interrupt usage on the MPC8572EAMC board.

Table 5-5. MPC8572E Interrupt Assignment

Name	Interrupt Source
INT0–2	Unused
INT3	Eth 0–4 PHYs
INT4	System CPLD

Table 5-5. MPC8572E Interrupt Assignment (continued)

Name	Interrupt Source
INT5	System CPLD
INT6-11	Unused

5.1.5 MPC8572E DUART1/2

The MPC8572E's DUART1/2 controller is used in conjunction with a FT2232D dual USB UART transceiver to implement two UART interfaces to one USB connector. External serial connection to the front panel of the card is made through a Mini-Type B USB connector. Figure 5-6 shows how the UART-USB serial connection is implemented on this design. (The #DEVID signal on the Mini-Type B USB connector is connected to a test point for debug purposes).

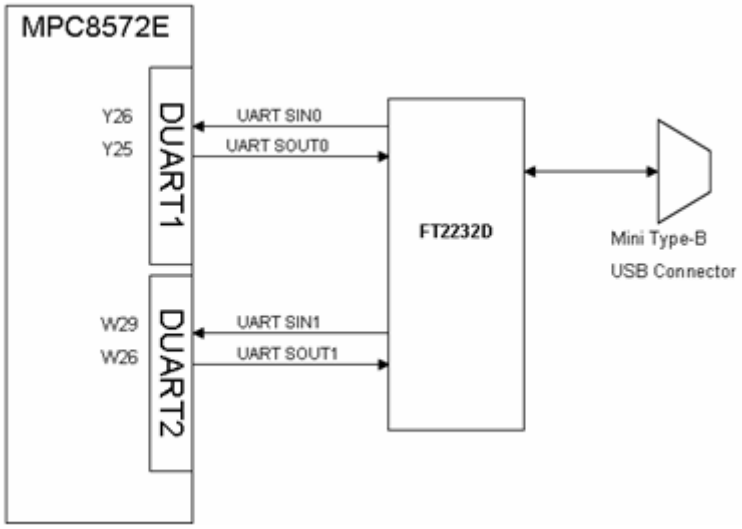

Figure 5-6. DUART Connectivity

NOTE

The USB/UART circuitry uses +5 V power generated within the MPC8572EAMC, and not that taken from the external +5 V device/supply.

5.1.6 COP/JTAG Debug Interface

In order to facilitate system testing, the MPC8572E provides a JTAG test access port (TAP) that complies with the IEEE 1149.1 boundary-scan specification. The common on-chip processor (COP) is part of the MPC8572E's JTAG machine and is implemented as an additional set of instructions/logic. The 16-pin JTAG port allows third party debug tools to be connected to the MPC8572E to allow extensive system debug. Table 5-6 shows the different signals on the COP/JTAG interface.

Table 5-6. COP/JTAG Interface Signals

Pin	Signal	Description
1	TDO	Transmit Data Out—MPC8572E's JTAG serial data output pin
2	NC	No Connect
3	TDI	Transmit Data in—MPC8572E's JTAG serial data input pin
4	TRST#	Test Port Reset. Used to reset the JTAG logic on the MPC8572E
5	+3.3 V	+3.3 V Power
6	+3.3 V	+3.3 V Power
7	TCLK	Test Port Clock. This clock is used to shift data in/out of the MPC8572E's JTAG logic.
8	CHK_STP_IN#	Check Stop In. This pin is pulled up to 3.3 V via a 10 k resistor.
9	TMS	Test Mode Select. This pin is used to change the state of the JTAG machine
10	NC	No Connect
11	SRESET#	Soft Reset. The MPC8572E's soft reset signal
12	NC	No Connect
13	HRESET#	Hard Reset. The MPC8572E's hard reset signal
14	NC	No Connect
15	CHK_STP_OUT#	Check Stop Out. This pin is pulled up to 3.3 V via a 10 k resistor.
16	GND	Digital ground

The MPC8572E's COP/JTAG interface can be accessed via a dedicated 16-pin header on the card itself. Figure 5-7 illustrates the connection between the AdvancedMC connector, Reset CPLD, 16-pin JTAG header, and the MPC8572E.

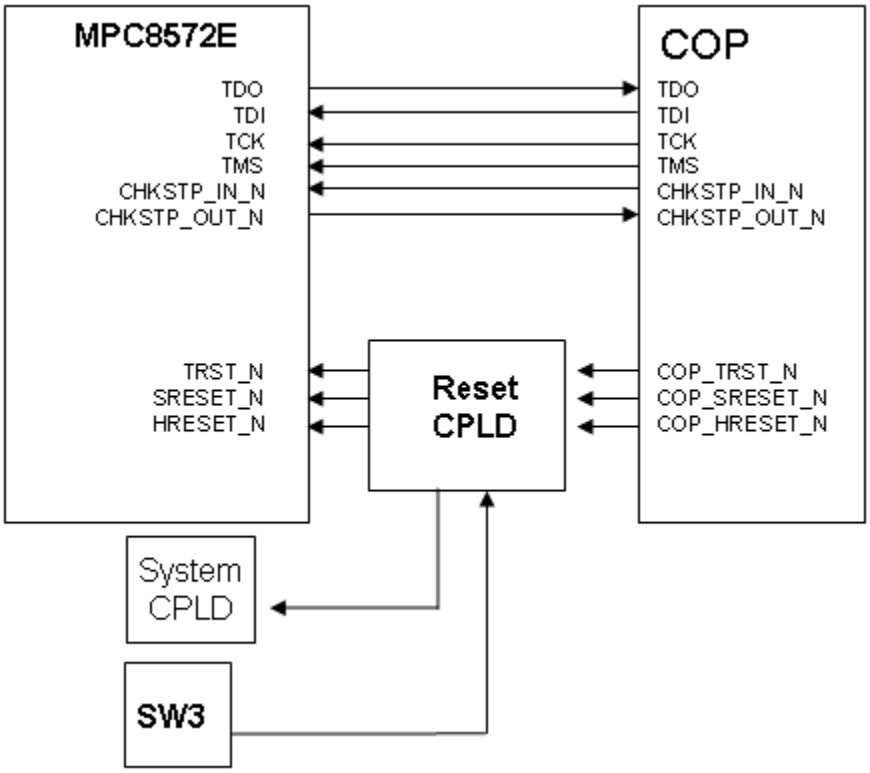

Figure 5-7. COP/JTAG Connectivity MPC8572EAMC

5.1.7 MPC8572E Power-On Reset Configuration (POR Config)

The power-on reset configuration of the PowerQUICC™ III family devices uses dedicated input pins that are sampled during the assertion of reset to configure the processor. The master reset signal is generated locally on-board from the reset circuitry, controlled by the System CPLD, as shown in Figure 5-8.

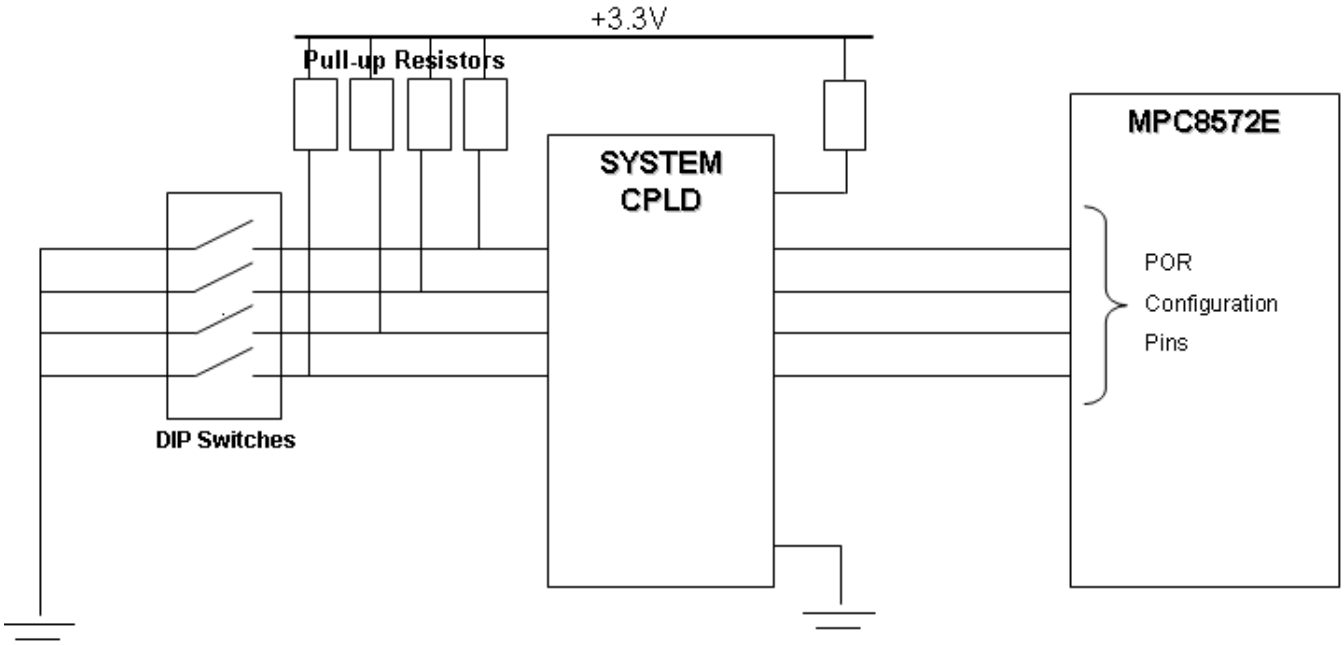

Figure 5-8. MPC8572E POR Configuration

All of the POR configuration signals are handled via System CPLD control. Some of the MPC8572EAMC signals are changeable via a set of DIP switches, whereas others are physically hard-wired on the board to minimize board space. Some of these signals have an internal pull-up that selects a default state. Table 5-7 details all POR configuration pins and their specific usage on the MPC8572EAMC board.

Table 5-7. MPC8572E POR Configuration DEFAULT Settings

POR Usage	Functional Pin (Reset Configuration Name)	Chip Default	Board Setting	Board Setup Description	Control Method
System PLL Ratio	LA[29:31] (cfg_sys_pll[0:2])	None	100	CCB Clock: SYSCLK Ratio = 10:1	DIP Switches
e500 Core0 PLL Ratio	LBCTL, LALE, LGPL2 (cfg_core0_pll[0:2])	None	100	E500 Core0: CCB Clock Ratio = 2:1	DIP Switches
e500 Core1 PLL Ratio	LWE[0], UART_SOUT[1], READY_P1 (cfg_core1_pll[0:2])	None	100	E500 Core1: CCB Clock Ratio = 2:1	DIP Switches
DDR PLL Ratio	TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 (cfg_ddr_pll[0:2])	None	100	DDR Complex CLK: DDRCLK Ratio = 10:1	DIP Switches
Boot ROM location	TSEC1_TXD[6:4],TSEC1_TX_ER (cfg_rom_loc[0:3])	1111	1111	Local Bus GPCM 32-bit ROM	DIP Switches

Table 5-7. MPC8572E POR Configuration DEFAULT Settings (continued)

POR Usage	Functional Pin (Reset Configuration Name)	Chip Default	Board Setting	Board Setup Description	Control Method
Host/Agent Config.	LWE[1:3]/LBS[1:3] (cfg_host_agt[0:2])	111	111	MPC8572E is root complex/ Host processor for all interfaces	DIP Switches
I/O Port Selection	TSEC1_TXD[3:1],TSEC2_TX_ER (cfg_IO_ports[0:3])	1111	1100	Serial RapidIO x4 (3.125 Gbps), 125-MHz reference clock	DIP Switches
CPU Boot Configuration	LA27,EC3_MDC (cfg_cpu0_boot, cfg_cpu1_boot)	11	10	Core #0 allowed to boot without waiting for external master; core #1 held in boot hold-off	DIP Switches
Boot Sequence Config.	LGPL3, LGPL5 (cfg_boot_seq[0:1])	11	11	Boot sequencer is disabled. No I^2C ROM is accessed	DIP Switches
DDR SDRAM Type	TSEC2_TXD[1] Cfg_dram_type	1	0	DDR-II 1.8 V, CKE low at reset	DDR2 only supported
FEC Configuration	DMA1_DDONE[1]_N (cfg_fec)	1	0	FEC Enabled, eTSEC3 and eTSEC4 are in SGMII mode	Fixed
eTSEC1 SGMII Mode	LA[28] (cfg_sgmii1)	1	0	eTSEC1 operates in SGMII mode	Fixed
eTSEC2 SGMII Mode	LGPL1 (cfg_sgmii2)	1	0	eTSEC2 operates in SGMII mode	Fixed
eTSEC3 SGMII Mode	TSEC3_TXD[3] (cfg_sgmii3)	1	0	eTSEC3 operates in SGMII mode	Fixed
eTSEC4 SGMII Mode	UART_SOUT[0] (cfg_sgmii4)	1	0	eTSEC4 operates in SGMII mode	Fixed
SGMII SerDes Ref Clock Configuration	TSEC_1588_TRIG_OUT (cfg_srds_sgmii_refclk)	1	1	SGMII Refclk = 125 MHz	Automatically selected based on SERDES configuration
eTSEC1 and eTSEC2 Width	EC1_MDC (cfg_tsec_1_reduce)	1	1	N/A—SGMII mode	Fixed
eTSEC3 and eTSEC4 Width	TSEC3_TXD[2] (cfg_tsec_3_reduce)	1	1	N/A—SGMII mode	Fixed
eTSEC1 Protocol	TSEC1_TXD[0], TSEC1_TXD[7] (cfg_tsec1_prtcl[0:1])	11	11	N/A—SGMII mode	Fixed
eTSEC2 Protocol	TSEC2_TXD[0], TSEC2_TXD[7] (cfg_tsec2_prtcl[0:1])	11	11	N/A—SGMII mode	Fixed
eTSEC3 Protocol	TSEC3_TXD[0], TSEC3_TXD[1] (cfg_tsec3_prtcl[0:1])	11	11	N/A—SGMII mode	Fixed
eTSEC4 Protocol	TSEC4_TXD[0], TSEC4_TXD[1] (cfg_tsec4_prtcl[0:1])	11	11	N/A—SGMII mode	Fixed

Table 5-7. MPC8572E POR Configuration DEFAULT Settings (continued)

POR Usage	Functional Pin (Reset Configuration Name)	Chip Default	Board Setting	Board Setup Description	Control Method
RapidIO Device ID	TSEC2_TXD[2:4] (cfg_device_ID[5:7])	None	000	Automatically configurable as host or slave device ID via System CPLD logic. If Host is set (current default) RIO device ID = 000, if Agent mode RIO device ID = 111. Other ID values possible via UBoot.	Automatically selected based on Host/Slave configuration
RapidIO System Size	LGPL0 (Config_rio_sys_size)	1	0	Large system size (up to 65535 devices)	DIP Switches
Memory Debug Configuration	DMA2_DACK[0],DMA1_DDONE[0] (cfg_mem_debug[0:1])	11	11	Debug information from the DDR SDRAM controller2 is driven on MSRCID and MDVAL	Fixed
DDR Debug Configuration	DMA2_DDONE[0] (cfg_ddr_debug)	1	1	Debug information is not driven on ECC pins.	Default assumed
General Purpose POR Configuration	LAD[0:31] (cfg_gpinut[0:31])	—	—	General-Purpose POR Configuration vector to be placed in GPPORCR	—
SerDes1 Enable	TSEC2_TXD[5] (cfg_srds1_en)	1	1	SerDes 1 Interface is enabled	Fixed
SGMII SerDes Enable	UART_RTS[1] (cfg_srds_sgmii_en)	1	1	SGMII SerDes Interface is enabled	Fixed
Engineering Use POR Configuration	MSRCID[0], MSRCID[1] (cfg_eng_use[0], cfg_eng_use[1])	—	—	—	—

5.2 MPC8572EAMC Ethernet Connectivity

The MPC8572E supports up to four Gigabit Ethernet ports. All four ports are configured in the SGMII mode to ease routing and reduce power on the MPC8572EAMC. As shown in Figure 5-9, two Marvell 88E1112 devices are used to provide the physical interfaces for the SGMII front panel Ethernet connectivity on the MPC8572EAMC board using eTSEC1 and eTSEC2. A further two 88E1112 devices are used to generate SGMII Ethernet functionality on the ports 0 and 1 of the rear AdvancedMC edge connector using eTSEC3 and eTSEC4 on the MPC8572E.

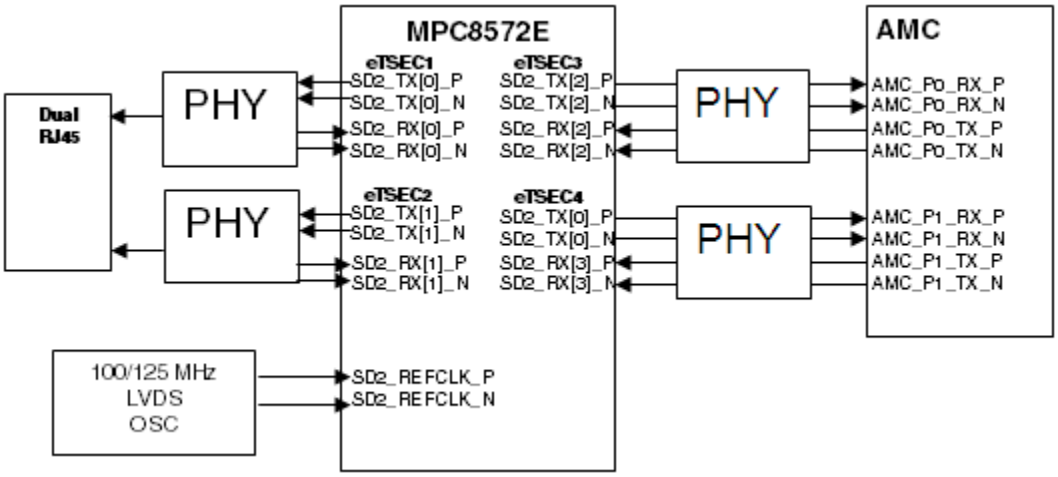

Figure 5-9. MPC8572E Gigabit Ethernet Connectivity

After reset, the initial power on status of each PHY is determined via six configuration pins: CONFIG[0:5], as shown in Table 5-8. These pins determine various initial setting such as the PHY address, clocking etc.

Table 5-8. 88E1112 PHY Configuration Pins

Pin	Bit[1]	Bit[0]
Config0	PHYADDR[1]	PHYADDR[0]
Config1	PHYADDR[3]	PHYADDR[2]
Config2	SGMII_CLK	PHYADDR[4]
Config3	SEL_TWSI	SEL_VTT
Config4	EEPROM[1]	EEPROM[0]
Config5	MODE[1]	MODE[0]

At power up, these configuration pins can be tied to VSS, VDDO or STATUS[1:0] in order to drive the correct configuration state. Table 5-9 details the pins used to set the values of the configuration pins.

Table 5-9. 88E1112 Pin Configuration Values

Pin	Bits [1:0]
VSS	0 0
STATUS[1]	0 1
STATUS[0]	1 0
VDDO	1 1

Table 5-10 shows the configuration settings for all four 88E1112 PHYs on the MPC8572EAMC.

Table 5-10. 88E1112 Reset Configuration Settings

Config	Configuration	Comments
Config_0	0 0	Address 0x00h, eTSEC1
Config_1	0 0	Address 0x00h
Config_2	0 0	SGMII Clock disabled, Address 0x00h
Config_3	0 0	MDC/MDIO, F/S_VTT internally regulated
Config_4	0 0	No EEPROM Read
Config_5	1 0	SGMII MAC interface to Copper, auto media select, such as FRONT PANEL
Config_0	0 1	Address 0x01h, eTSEC2
Config_1	0 0	Address 0x01h
Config_2	0 0	SGMII Clock disabled, Address 0x01h
Config_3	0 0	MDC/MDIO, F/S_VTT internally regulated
Config_4	0 0	No EEPROM Read
Config_5	1 0	SGMII MAC interface to Copper, auto media select, such as FRONT PANEL
Config_0	1 1	Address 0x03h, eTSEC3
Config_1	0 0	Address 0x03h
Config_2	0 0	SGMII Clock disabled, Address 0x03h
Config_3	0 0	MDC / MDIO, F/S_VTT internally regulated
Config_4	0 0	No EEPROM Read
Config_5	1 1	SGMII MAC interface to 1000Base-X, auto media select, such as AdvancedMC BACKPLANE
Config_0	0 0	Address 0x04h, eTSEC4
Config_1	0 1	Address 0x04h
Config_2	0 0	SGMII Clock disabled, Address 0x04h
Config_3	0 0	MDC/MDIO, F/S_VTT internally regulated

Table 5-10. 88E1112 Reset Configuration Settings (continued)

Config	Configuration	Comments
Config_4	0 0	No EEPROM Read
Config_5	1 1	SGMII MAC interface to 1000Base-X, auto media select, such as AdvancedMC BACKPLANE

Therefore, front panel eTSEC1 Gigabit Ethernet has physical address 0x00h and eTSEC2/3/4 have addresses 0x01h, 0x03h, and 0x04h, respectively. eTSEC1 and eTSEC2 are configured as SGMII copper interfaces, and eTSEC3 and eTSEC4 are both configured as an SGMII fiber interface.

The last Ethernet interface used on the MPC8572EAMC is generated using Marvell's 88E3018 PHY. Using hardware configuration pins, this 10/100BaseT PHY is configured in much the same way as the 88E1112 PHYs that have just been discussed. The 88E3018 is configured using four configuration bits and a three bit control word as shown in Table 5-11.

Table 5-11. 88E3018 PHY Configuration Pins

Pin	Bit[2]	Bit[1]	Bit[0]
Config0	RES	PHYADDR[1]	PHYADDR[0]
Config1	RES	PHYADDR[3]	PHYADDR[2]
Config2	RES	ENA_XC	PHYADDR[4]
Config3	MODE[2]	MODE[1]	MODE[0]

The 88E3018 PHY uses the VSS, LED[0:2], CRS, COL and VDDO pins to drive different hardware configuration words onto pins during power up. Table 5-12 details the pins used to set the values of the 88E3018's configuration pins.

Table 5-12. 8E3018 Pin Configuration Values

Pin	Bits[2:0]
VSS	0 0 0
LED[0]	0 0 1
LED[1]	0 1 0
LED[2]	0 1 1
CRS	1 0 0
COL	1 1 0
VDDO	1 1 1

Table 5-13 shows how the 88E3018 PHY device is configured and physically addressed. Therefore, the front panel 10/100 Ethernet debug port has physical address 0x02h.

Table 5-13. 88E3018 Reset Configuration Settings

Config_0	0 1 0	Address 0x02h, FEC
Config_1	0 0 0	Address 0x02h
Config_2	0 1 0	Enable X-over, PHY AD4 = 0
Config_3	0 1 1	Copper MII

5.3 Clocking

All clocks used on the MPC8572EAMC are generated locally using crystal oscillators. The only exception is the PCI-Express clock, which can be generated either locally (using a 100-MHz crystal oscillator), or externally using the FCLKA input pins (pins 80 and 81 on the AdvancedMC connector). This clock selection is controlled via the System CPLD logic. A number of different clocking schemes are used on the MPC8572EAMC, as follows:

- MPC8572EAMC System clock, SYSTEM CPLD, DDR Clock (66.66 MHz)
- MPC8572E Real Time Clock (16 MHz)
- 10/100 Ethernet PHY, SGMII Gigabit Ethernet PHY Clock (25 MHz)
- Reset CPLD Clock, MMC (ColdFire 5213) Clock (9.8304 MHz)
- SERDES Clock (100/125 MHz)

5.3.1 MPC8572EAMC System Clock (SYSCLK)

The system clock is provided by a 66.66-MHz crystal oscillator. This clock is fed through a 22 Ω series resistor to produce the required processor system clock, as shown in Figure 5-10.

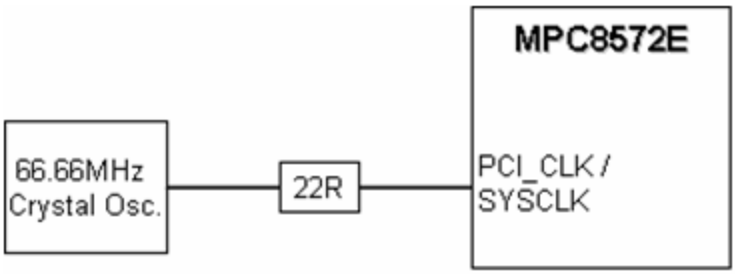

Figure 5-10. SYSCLK Configuration

5.3.2 MPC8572EAMC Real Time Clock (RTC)

A 16-MHz crystal is used to produce the RTC clock input. Figure 5-11 illustrates how the RTC is configured on the MPC8572EAMC. Users should note that the 16-MHz crystal oscillator is not populated on the MPC8572EAMC. The real time clock can either be used locally on board (by populating the 16-MHz crystal), or the System CPLD logic can be programmed to allow the RTC to drive the RTC externally onto one of the AdvancedMC clock pins (such as FCLKA/TCLKA-D).

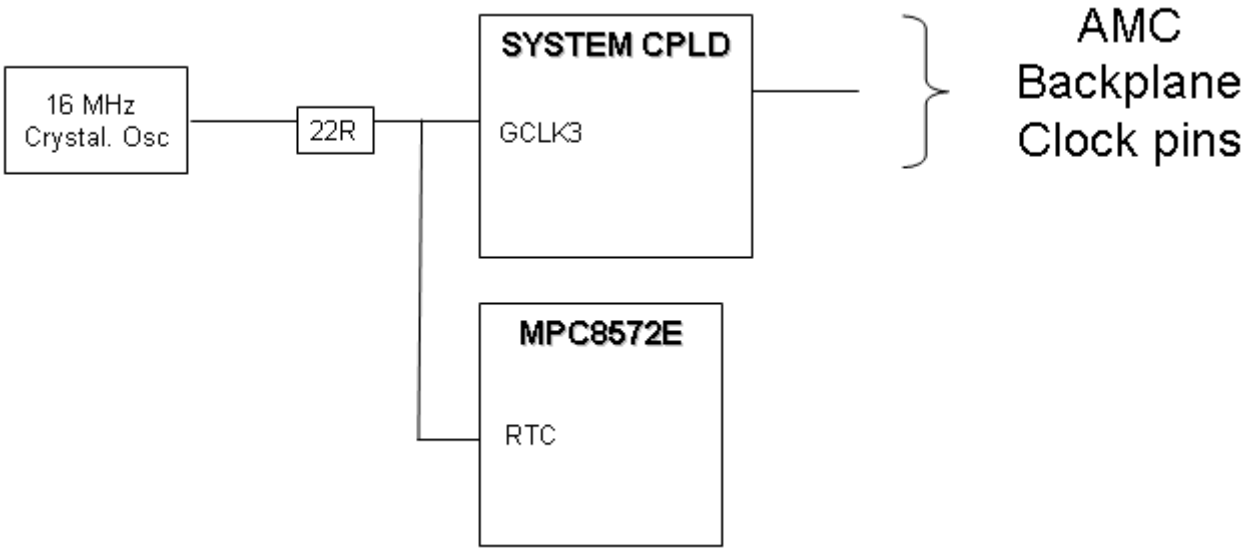

Figure 5-11. RTC Configuration

5.3.3 MPC8572EAMC DDR Clock (DDRCLK)

The DDRCLK can be used to separately clock the DDR interface, rather than the main CCB clock. A 66.66-MHz crystal is used to produce the DDRCLK clock input as shown in Figure 5-12.

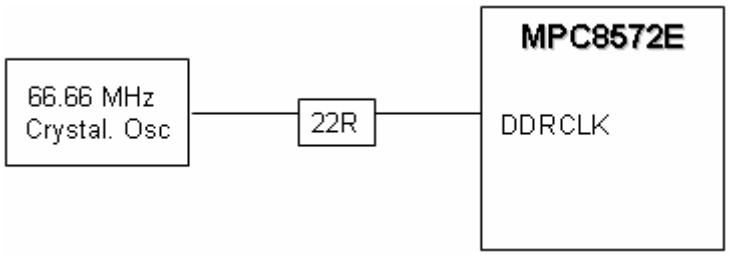

Figure 5-12. DDRCLK Configuration

5.3.4 SGMII Gigabit Ethernet PHY Clocks

The MPC8572EAMC has four SGMII Gigabit Ethernet interfaces. In order to minimize on PCB floor space, a single 25-MHz crystal is fed into an IDT ICS524, low skew 1:4 clock buffer. This is illustrated in Figure 5-13.

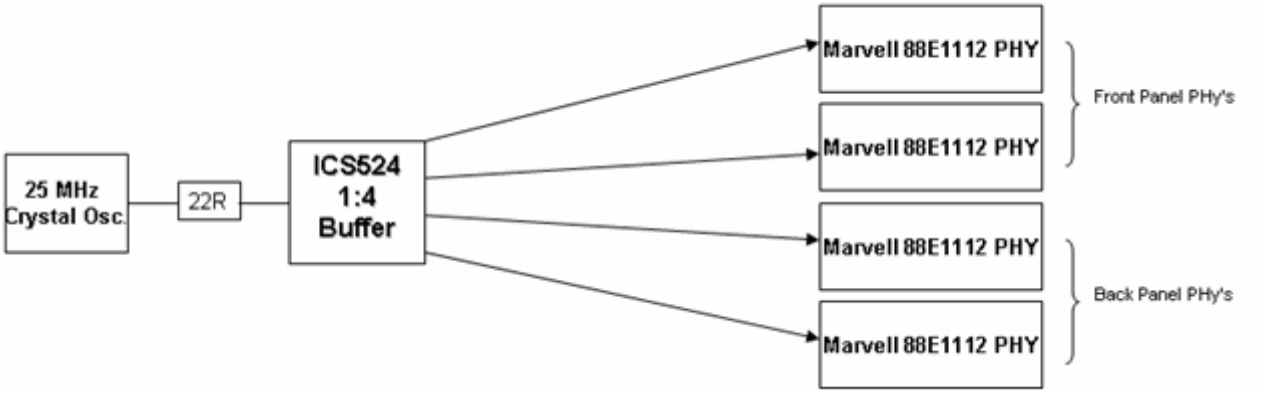

Figure 5-13. SGMII Ethernet Clock Configuration

5.3.5 FEC 10/100 Ethernet PHY Clock

A single 25-MHz crystal oscillator and 22 Ω series resistor is used to provide the input clock to the Marvell 88E3018 PHY, shown in Figure 5-14.

Figure 5-14. FEC Ethernet Clock Configuration

5.3.6 MMC Clock—ColdFire MCF5213 (EXTAL)

The AdvancedMC Module Management Controller uses a ColdFire MCF5213 to provide card management control requires a 9.8304-MHz clock source as shown in Figure 5-15.

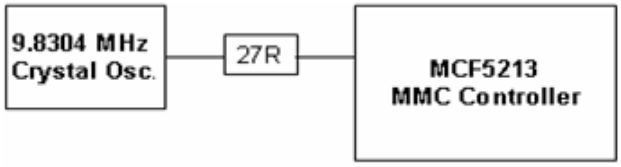

Figure 5-15. MMC (MCF5213) Clock Configuration

5.3.7 MPC8572EAMC SERDES LVDS Clock (100/125MHZ)

The MPC8572E microprocessor has integrated support for both PCI-Express and Serial RapidIO. To support both PCI-E and SRIO standards, two high precision crystal oscillators are used, 100 MHz and 125 MHz. The AdvancedMC standard also requires that common clocking is supported via the fabric clock interface, FCLKA. Figure 5-16 illustrates how the ICS854054 fan-out buffer connects to the three differential clock input sources.

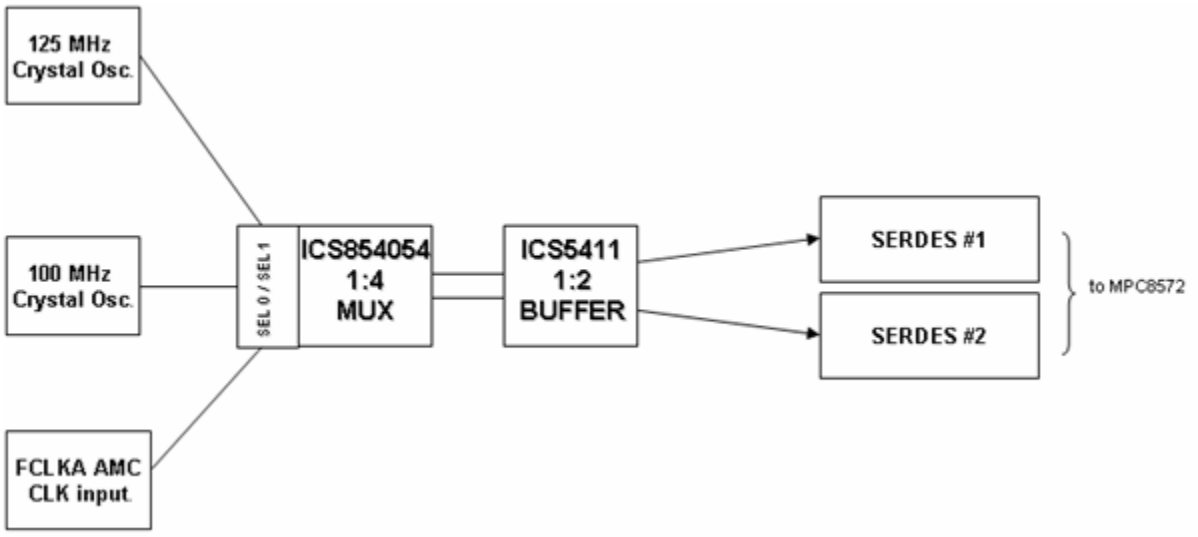

Figure 5-16. SERDES 100/125MHZ/FCLKA Clock Configuration

Table 5-14 shows the truth table for the ICS854054 device. The selected differential LVDS clock output is then fed into an ICS85411, 1-to-2 Differential-to-LVDS fan-out buffer. This buffer splits the LVDS input clock out to the two SERDES interfaces on the MPC8572E. This logic is automatically handled by the System CPLD logic.

Table 5-14. ICS854054 Truth Table

Inputs		Outputs		
SEL1	SEL0	Q	nQ	
0	0	PCLK0	nPCLK0	125 MHz
0	1	PCLK1	nPCLK1	100 MHz
1	0	PCLK2	nPCLK2	FCLKA
1	1	PCLK3	nPCLK3	Unused

5.3.8 MPC8572EAMC Clock Port Region

The AdvancedMC clock port region is located on pins 74 through 82 on the AdvancedMC edge connector. Differential synchronization clock 1 on pins 74/75, differential synchronization clock 2 on pins 77/78 and differential synchronization clock 1 on pins 80/81. The AdvancedMC specification dictates that two types of optional clock sources are provided to/from the board: four Telecom clocks and one Fabric clock. The

GPCLK1 and GPCLK2 pins on the CPLD (J5 and J12) are used to receive TCLK1 and TCLK3 into the AdvancedMC module.

The DS90LV028A Dual CMOS Differential Line Receiver is used to convert both TCLK1 and TCLK3 into single ended TTL clocks. A DS90LV049, LVDS Dual Line Driver with Dual Line Receiver is used to convert between single ended differentials. 100-Ω resistors are required at both the output terminals of the DS90LV049 in order to correctly terminate the clock signals. Clocking schemes of both the DS90LV049 and DS90LV028A are shown in Figure 5-17.

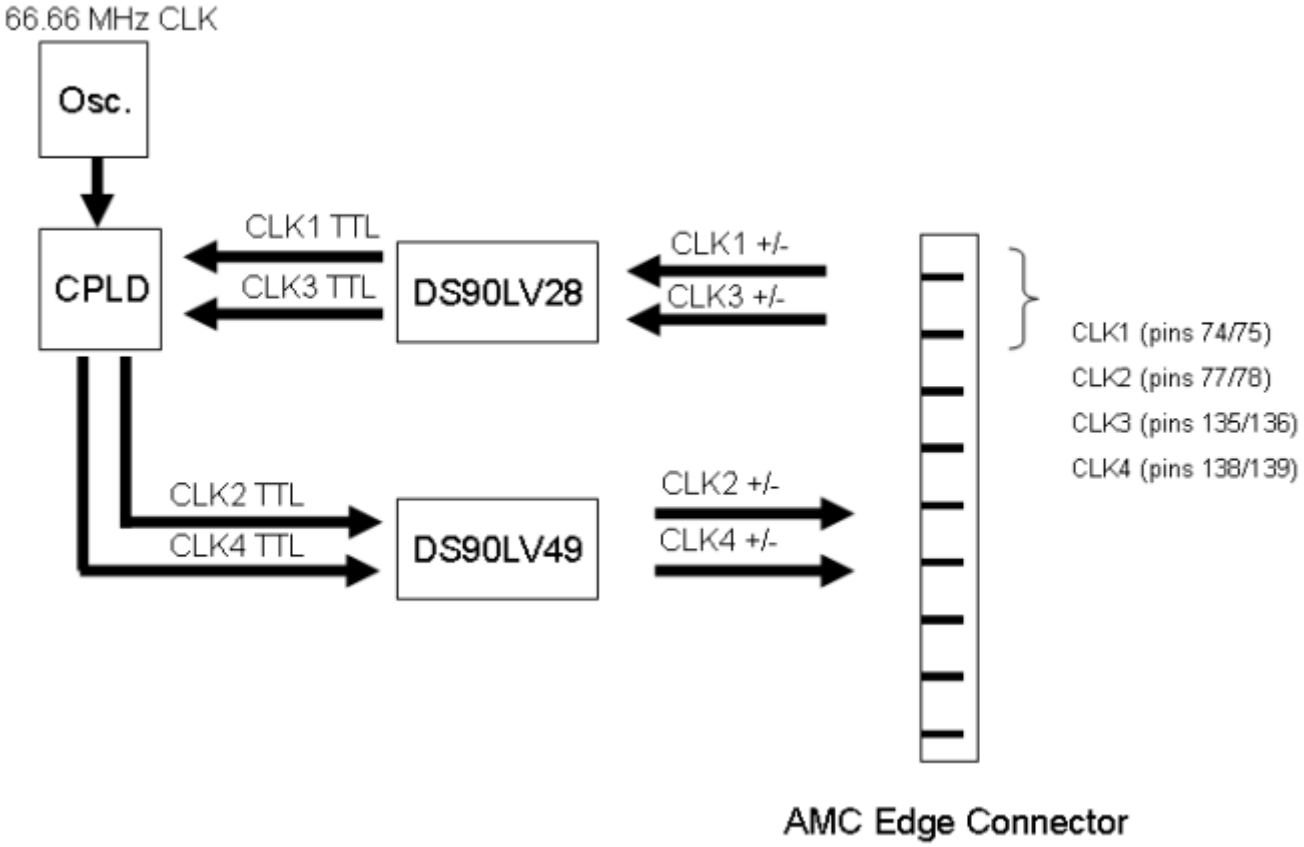

Figure 5-17. AdvancedMC Clock Port Region

5.4 General Board Configuration

The following subsections describe general board configuration.

5.4.1 MPC8572EAMC Power

Two separate power rails are available on the card, as follows:

- Management Power—Typically 3.3 V (150 mA maximum), used to power MMC circuitry
- Payload Power—Typically 12 V, (5.85 A maximum), used to power the rest of the board

All of the required voltages for the card are generated locally on board from these 12 V and 3.3 V power supplies. Several smaller power modules use this 12 V intermediate bus to generate the required voltages.

5.4.1.1 MPC8572EAMC Voltage Requirements

The MPC8572EAMC has a number of on-board peripheral chips, each with its own voltage and power requirements. To determine a safe power budget for the MPC8572EAMC, the power characteristics of each device must be determined. Table 5-15 highlights the main peripheral chips used on the MPC8572EAMC and their individual voltage/power requirements.

Table 5-15. MPC8572EAMC Power Requirements

Device Name	MPC8572EAMC Section	Supply Voltage (V)	Supply Current (mA)	Power (W)	Temp Range (C)	Comments
S29GL512N	Local Bus	3.3	100	0.33	–40–85	Tabulated values are 2x (2 devices on board)
SN74LV32973	Local Bus	3.3	0.12	0.386	–40–85	Tabulated values are 2x (2 devices on board)
VL491T2863T-E6	DDR	1.8V Generated from 5.0 V	4720	8.5	–20–125	Tabulated values are 2x (2 devices on board).
TPS51116	DDR	5.0	702	3.51	–40–85	—
125/100MHz	Clocking	3.3	150	1.65	–40–85	Tabulated values are 2x (2 devices on board)
ICS85411	Clocking	3.3	25	0.0825	–40–85	—
ICS854054	Clocking	3.3	61	0.201	–40–85	—
ICS524	Clocking	3.3	25	0.0825	–40–85	—
88E3018	10/100 Ethernet	2.5	90 + 5 + 8	2.575	–40–85	Tabulated values are for AVDD, AVDDC, VDDO
88E3018	10/100 Ethernet	1.2	40	0.1	–40–85	Tabulated values are for DVDD
0826-1X1T-43-F	10/100 Ethernet	2.5	40	0.1	–40–85	—
88E1112 Backplane	Ethernet	2.5	(20 + 14 + 28 + 49) × 2 = 222	0.555	–40–85	Tabulated values are 2x (2 devices on board)
88E1112 1000BaseT	Ethernet	2.5	(14 + 28 + 46 + 142 + 106) × 2 = 672	1.68	–40–85	Tabulated values are 2x (2 devices on board)
MPC8572E Core	Processor	1.1	20450	22.5	0–70	—

All of the above MPC8572EAMC voltages are provided using Power-One and Maxim voltage regulators. Both of these manufacturers have voltage regulators that operate off of the 12-V payload power, or from the generated 3.3-V supply.

5.4.1.2 Power Supply Distribution

Figure 5-18 shows the power distribution used on the MPC8572EAMC.

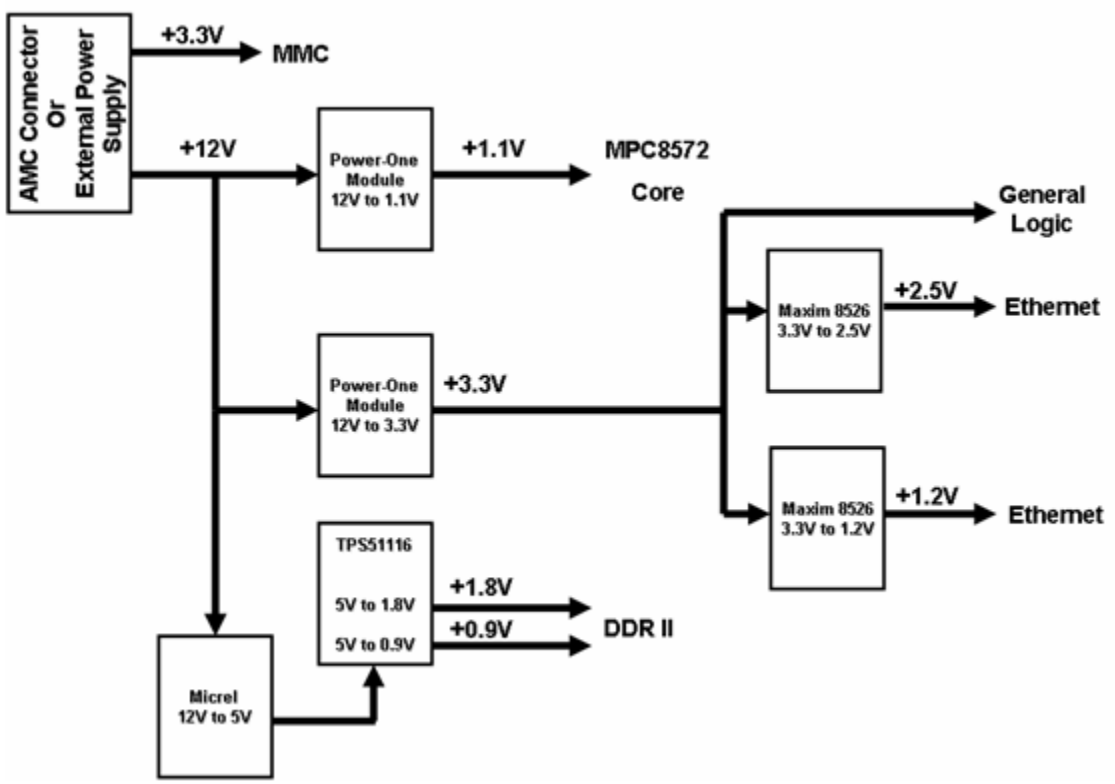

Figure 5-18. MPC8572EAMC Power Distribution

The board receives IPMCV (3.3 V), 12 V, and ground from the AdvancedMC edge connector. The 12 V is fed to three DC-DC power modules. Two Power-One modules separately generate the 1.1 V core and 3.3 V IO supply voltages. The TPS51116 voltage regulator is designed exclusively for use with the DDRII memory. This device generates the power and reference supply for the two DDR2 SoCDIMMs. Two Maxim MAX8526 devices are used to generate additional 2.5 V and 1.2 V board power supplies. A single Micrel MIC5205 device is used to provide the 5 V power supply for the TPS51116 device and the FT2232D dual USB controller, generated from the 12 V AdvancedMC supply.

5.4.1.3 Voltage Regulator Configuration

The Power-One voltage regulators have user selectable output voltages defined using trim resistors. The following equation is used to calculate the correct output voltage.

$$R_{TRIM} = \frac{10.5}{(V_{O\text{-}REQ} - 0.7525)} - 1 \qquad [k\Omega]$$

Using this equation, a trim resistor value of 29.2 kΩ is required on the Power-One YNC12S20 device (1.1-V voltage regulator). (As this is not a standard resistor value, two parallel resistors (43 kΩ//91 kΩ)

generate a combined resistance of 29.201 kΩ = 1.1001 V). Similarly, the Power-One YM12S05 (3.3 V voltage regulator) requires a trim resistor of 3.12 kΩ. (A parallel resistor combination (3.3 kΩ//59 kΩ) is used to create a resistance value of 3.125 kΩ. This gives an output voltage of 3.298 V).

The Maxim MAX8526 device also has a configurable output voltage that uses a similar resistor arrangement to select the desired output voltage. Manufacturers guidelines recommend VFB = 0.5 V and R2 < 5 kΩ in order to optimize quiescent current, accuracy, and high-frequency power-supply rejection. R2 is chosen to be 4.7 kΩ. Selection of the desired output voltage is given using the following equations.

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right) \qquad R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

Substituting these values into the equations above for Vout values of 2.5 and 1.2 V yields: 2.5 V = 18.8 kΩ, 1.2 V = 6.58 kΩ. Using standard resistance values, the closest resistors are 18.7 kΩ and 6.98 kΩ respectively. Table 5-16 summarizes the trim resistors required for the Power-one and Maxim devices on the MPC8572EAMC.

Table 5-16. Voltage Regulation/Device Parameters

PSU Voltage	Manufacturer	Vout (V)	Trim Resistor (kΩ)	Trim Resistor Standard Value (kΩ)	Vout Actual (V)
3.3	Power-One—YM12S05	3.3	3.122 kΩ	3.3 kΩ//59 kΩ	3.298
2.5	Maxim—MAX8526	2.5	R1 = 18.7 kΩ R2 = 4.7 kΩ	R1 = 18K7	2.489
1.2	Maxim—MAX8526	1.2	R1 = 6.98 kΩ R2 = 4.99 kΩ	R1 = 6.57 kΩ	1.198
1.1	Power-One—YNC12S20	1.1	29.216 kΩ	43 kΩ//91kΩ	1.1001

The MPC8572E requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. VDD, AVDD_*n*, BVDD, SCOREVDD, LVDD, TVDD, XVDD, OVDD
2. GVDD

All supplies must be at their stable values within 50 ms. Correct power rail sequencing is achieved by via CPLD control.

5.4.1.3.1 MPC8572EAMC Board Headers

The MPC8572EAMC has a number of headers placed on the board for debug, control, IO and peripheral functions such as fan cooling and power etc. Header 1 is the COP/JTAG interface used for debug and control of the main MPC8572E processor. Table 5-17 details the configuration of this header.

Table 5-17. J6—MPC8572E COP/JTAG Interface

Pin #	Signal	Description
1	TDO	Transmit data out—MPC8572E's JTAG serial data output pin
2	NC	No Connect
3	TDI	Transmit Data in - MPC8572E's JTAG serial data input pin
4	TRST#	Test Port Reset. Used to reset the JTAG logic on the MPC8572E
5	+3.3 V	+3.3 V Power
6	+3.3 V	+3.3 V Power
7	TCLK	Test Port Clock. This clock is used to shift data in/out of the MPC8572E's JTAG logic
8	CHK_STP_IN#	Check Stop In. This pin is pulled up to 3.3 V via a 10 k resistor
9	TMS	Test Mode Select. This pin is used to change the state of the JTAG machine
10	NC	No Connect
11	SRESET#	Soft Reset. The MPC8572E's soft reset signal
12	NC	No Connect
13	HRESET#	Hard Reset. The MPC8572E's hard reset signal
14	NC	No Connect
15	CHK_STP_OUT#	Check Stop Out. This pin is pulled up to 3.3 V via a 10 k resistor
16	GND	Digital ground

The MPC8572EAMC has a second 10-pin JTAG interface that is used for controlling the CPLD logic. This interface is detailed in Table 5-18.

Table 5-18. HD1—Reset/System CPLD JTAG Interface

Pin #	Signal	Description
1	TCLK	Test port clock. This clock is used to shift data in/out of the CPLD's JTAG logic.
2	NC	No Connect
3	TMS	Test Mode Select. This pin is used to change the state of the JTAG machine
4	GND	Digital Ground
5	TDI	Transmit Data in—CPLD's JTAG serial data input pin
6	VCC	+3.3 V Power
7	TDO	Transmit Data Out—CPLD's JTAG serial data output pin
8	GND	Digital Ground

Table 5-18. HD1—Reset/System CPLD JTAG Interface (continued)

Pin #	Signal	Description
9	NC	No Connect
10	NC	No Connect

The module management controller (MMC) is based around the ColdFire MCF52134. This device has a background debugger mode (BDM) connector. The pins out of this 16-way connector are detailed in Table 5-19.

Table 5-19. J1—MCF5213 BDM Interface

Pin #	Signal	Description
1	NC	No connect.
2	CF_TMS	Test Mode Select. This pin is used to change the state of the BDM machine
3	GND	Digital ground
4	CF_TRST_B#	Test Port Reset. Used to reset the BDM logic on the MCF5213
5	GND	Digital ground
6	CF_TCLK	Test Port Clock. This clock is used to shift data in/out of the MCF5213's BDM logic
7	CF_RESET_HDR#	This signal is used to reset the BDM logic
8	CF_TDI	Transmit Data in – MCF5213's JTAG serial data input pin
9	IPMI	+3.3V Power
10	TDO	Transmit Data Out – MPC8572E's JTAG serial data output pin
11	GND	Digital ground
12	CF_ALLPST	Logical AND of PST0 ... PST3 core status signals. Allows a debugger to know whether the core is running or halted.
13	CF_ALLPST	Logical AND of PST0 ... PST3 core status signals. Allows a debugger to know whether the core is running or halted.
14	CF_ALLPST	Logical AND of PST0 ... PST3 core status signals. Allows a debugger to know whether the core is running or halted.
15	CF_ALLPST	Logical AND of PST0 ... PST3 core status signals. Allows a debugger to know whether the core is running or halted.
16	NC	No Connect

To examine the debug information from the MMC the UART output from the MCF5213 is connected via an RS-232 transceiver to the 3-way header, J2. Table 5-20 shows the different pin connections of this header.

Table 5-20. J2—MCF5213 Serial Interface

Pin #	Signal	Description
1	TXD	Serial Transmit Data output
2	RXD	Serial Receive Data input
3	GND	Digital ground

To assist with CPLD debug and system bring-up a specific header is used to include or isolate the System CPLD from the AdvancedMC JTAG chain. Table 5-21 illustrates the pin connections of this interface.

Table 5-21. J12—CPLD Debug Interface

Pin #	Signal	Description
1	CPLD_TDO	JTAG TDO from CPLD
2	RESET_TDO	JTAG TDO from Reset CPLD
3	SYSTEM_TDO	JTAG TDO from System CPLD

5.4.2 Board CPLD Logic/POR Configuration

The Reset CPLD is a critical component on the MPC8572EAMC design. This device is responsible for providing the following functions:

- Generating a board reset signal
- Synchronizing all CPLD signals to the input CPLD clock
- Checking the presence of a 12-V power supply
- Powering up all board power supplies (in the correct sequence)
- Bringing up all devices out of reset (in the correct sequence)
- Giving the System CPLD a “go” to start the POR Config cycles

The Reset CPLD is based around the Altera EPM240T100C5N device. The internal operation of this Reset CPLD is factory programmed and is reserved for factory use only.

The Altera MaxII EPM1270 System CPLD is responsible for reset, POR configuration of the MPC8572E, signal fan-out, logic/pin multiplexing, COP/JTAG control (of the CPLD itself, the AdvancedMC JTAG and MPC8572E JTAG signals). One of the main methods by which a user can configure the board is through the use of three on-board DIP switches. These switches are read by the System CPLD during the MPC8572E’s POR configuration cycle phase. The function of these DIP switches is detailed in the tables below. The following table syntax is used:

“0” implies a logic low. This is achieved by turning the switch on.

“1” implies a logic high. This is achieved by turning the switch off.

Switch 5 is used to configure the system clocks of both cores of the MPC8572E and boot ROM location, shown in Table 5-22.

Table 5-22. SW5—System Clocks/Boot Location

Switch Position	Configuration Settings	Description (ON=0, OFF=1)
1-20	System PLL Ratio CCB: Sysclk [CCB1:CCB0]	0: 4:1 0 1: 8:1 1 0: 10:1 1 1: 12:1
3-4	e500 Core Clock Ratio e500 core 0: CCB [e500Ratio1:e500Ratio0]	0 0: 1.5:1 0 1: 2:1 1 0: 2.5:1 1 1: 3.5:1
5-6	e500 Core Clock Ratio e500 core 1: CCB [e500Ratio1:e500Ratio0]	0 0: 1.5:1 0 1: 2:1 1 0: 2.5:1 1 1: 3.5:1
7-8	Boot ROM Location	0 0: Boot ROM in PCIe 0 1: Boot ROM in SRIO 1 0: Boot ROM in DDR 1 Controller 1 1: GPCM Local Bus Controller (32-bit ROM)

Switch 500 is used to configure the DDR clock ratio, host/agent and PCI/Serial RapidIO configuration, shown in Table 5-23.

Table 5-23. SW500—DDR Clock Ratio/SERDES/Host-Agent Mode

Switch Position	Configuration Settings	Description (ON = 0, OFF = 1)
1-3	DDRCLK PLL Ratio	0 0 0: DDR PLL ratio 3:1 0 0 1: DDR PLL ratio 4:1 0 1 0: DDR PLL ratio 6:1 0 1 1: DDR PLL ratio 8:1 1 0 0: DDR PLL ratio 10:1 1 0 1: DDR PLL ratio 12:1 1 1 0: DDR PLL ratio 14:1 1 1 1: DDR Synchronous Mode
4-5	Host/Agent Configuration	0 0: MPC8572E acts as agent of every interface 0 1: MPC8572E acts as an agent of a PCI Express host 1 0: MPC8572E acts as an endpoint of a PCI Express /SRIO host 1 1: MPC8572E acts as the host processor
6-8	SERDES Configuration	0 0 0: PCI-E x4 (2.5Gbps); 100MHz ref clock 0 0 1: Serial RapidIO x4 (2.5Gbps); 100MHz ref clock 0 1 0: Serial RapidIO; PCI-E x4 (2.5Gbps); 100MHz ref clock 0 1 1: Serial RapidIO; PCI-E x4 (1.25; 2.5Gbps); 100MHz ref clock 1 0 0: Serial RapidIO x4 (3.125Gbps) 125MHz ref clock 1 0 1: Serial RapidIO x4 (1.25Gbps) 100MHz ref clock 1 1 0: Serial RapidIO x4 (1.25Gbps) 100MHz ref clock 1 1 1: Serial RapidIO x4 (1.25Gbps) 100MHz ref clock

Switch 501 is used to determine whether the I2C boot sequencer is enabled or disabled and how both of the dual cores boot, shown in Table 5-24. Finally, bit 4 selects the size of the Serial RapidIO system.

Table 5-24. SW501—CPU Boot/Boot Sequencer Mode/System Size

Switch Position	Configuration Settings	Description (ON = 0, OFF = 1)
1	BOOT Sequencer Configuration	0: Normal I2C Addressing Mode 1: Boot Sequencer Disabled
2-3	CPU BOOT Configuration	00: CPU boot hold off, both cores 01: E500 core #1 boots, core #0 in hold-off 10: E500 core #0 boots, core #1 in holdoff 11: Both cores boot without external master
4	Serial RapidIO System Size Configuration	0: Large system < 65536 devices 1: Small system < 256 devices

5.5 AdvancedMC Backplane Connector

The MPC8572EAMC is compatible to the AMC.0 specification. The AMC.0 specification defines the layout/pin-out of the AdvancedMC edge connector that is used to connect to the carrier card. The edge connector is sub-divided into four distinct port regions:

- Clocks—The synchronization clock interface
- Common Options—Support for essential interfaces which are common across multiple Fat Pipe Implementations
- Fat Pipes Region—Provides support for the data path
- Extended Options—Recommended to be used by the Rear Transition Module (RTM), or as an extension to the Common Options, or fat Pipe Region if required

The current AMC.2 (XAUI) specification places the first XAUI link at ports 8–11, and the second link at ports 4–7. However, the current AMC.4 (SRIO) specifications place the first Serial RapidIO link at ports 4–7, and the second at 8–11 (such as, opposite the latest AMC.2 specification). Scope Analysis of the port mappings recommend that AMC.4 also provides the first Serial RapidIO ports on 8–11, consistent with AMC.2. In order to support legacy port mappings and the new Scope recommendations, AdvancedMC port configuration resistors can be soldered to allow both configurations to be met. See Figure 5-2.

Figure 5-19 gives a summary of the port signal mapping of the AdvancedMC connector.

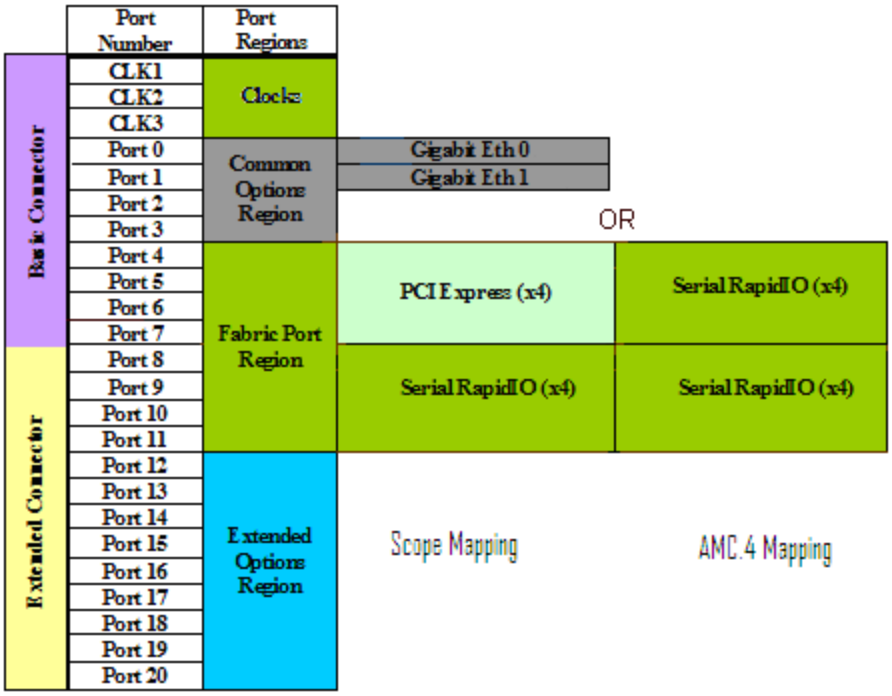

Figure 5-19. MPC8572EAMC, AdvancedMC Connector Signal Mapping

The following two tables illustrate the physical connections to the AdvancedMC edge connector. Table 5-25 shows the carrier AdvancedMC site pin definition component (side 1—required half) and Table 5-26 the carrier AdvancedMC site pin definition component (side 2—optional half).

Table 5-25. Carrier AdvancedMC Site Pin Definitions (Side 1—Required Half)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
01	GND	—	First	—	GND
02	+12 V	—	First	—	+12 V
03	PS1#	—	Last	—	PS1#
04	MP	—	First	—	+3.3 V
05	GA0	Carrier	Second	Carrier	GA0
06	RSRVD	Module	Second	—	NC
07	GND	—	First	—	GND
08	RSRVD	Carrier	Second	—	NC
09	+12 V	—	First	—	+12 V
10	GND	—	First	—	GND

Table 5-25. Carrier AdvancedMC Site Pin Definitions (Side 1—Required Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
11	TX0+	Module	Third	Module	AMC_PORT_0_RX_P
12	TX0–				AMC_PORT_0_RX_N
13	GND	—	First	—	GND
14	RX0+	Carrier	Third	Carrier	AMC_PORT_0_RX_P
15	RX0–				AMC_PORT_0_RX_N
16	GND	—	First	—	GND
17	GA1	Carrier	Second	—	GA1
18	+12 V	—	First	—	+12 V
19	GND	—	First	—	GND
20	TX1+	Module	Third	—	AMC_PORT_1_RX_P
21	TX1–			—	AMC_PORT_1_RX_N
22	GND	—	First	—	GND
23	RX1+	Carrier	Third	—	AMC_PORT_1_RX_P
24	RX1–			—	AMC_PORT_1_RX_N
25	GND	—	First	—	GND
26	GA2	—	Second	Carrier	GA2
27	+12 V	—	First	—	+12 V
28	GND	—	First	—	GND
29	TX2+	Module	Third	Module	NC
30	TX2–				
31	GND	—	First	—	GND
32	RX2+	Carrier	Third	Carrier	NC
33	RX2–				
34	GND	—	First	—	GND
35	TX3+	Module	Third	—	NC
36	TX3–			—	
37	GND	—	First	—	GND
38	RX3+	Carrier	Third	—	NC
39	RX3–			—	
40	GND	—	First	—	GND
41	ENABLE #	—	Second	—	ENABLE #

Table 5-25. Carrier AdvancedMC Site Pin Definitions (Side 1—Required Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
42	+12 V	—	First	—	+12 V
43	GND	—		—	GND
44	TX4+	Module	Third	Module	AMC_PORT4_TX_P
45	TX4–				AMC_PORT4_TX_N
46	GND	—	First	—	GND
47	RX4+	Carrier	Third	Carrier	AMC_PORT4_RX_P
48	RX4–				AMC_PORT4_RX_N
49	GND	—	First	—	GND
50	TX5+	Module	Third	—	AMC_PORT5_TX_P
51	TX5–			—	AMC_PORT5_TX_N
52	GND	—	First	—	GND
53	RX5+	Carrier	Third	—	AMC_PORT5_RX_P
54	RX5–			—	AMC_PORT5_RX_N
55	GND	—	First	—	GND
56	SCL_L	IPMI Agent	Second	—	I2C
57	+12 V	—	First	—	+12 V
58	GND	—		—	GND
59	TX6+	Module	Third	—	AMC_PORT6_TX_P
60	TX6–			—	AMC_PORT6_TX_N
61	GND	—	First	—	GND
62	RX6+	Carrier	Third	—	AMC_PORT6_RX_P
63	RX6–			—	AMC_PORT6_RX_N
64	GND	—	First	—	GND
65	TX7+	Module	Third	—	AMC_PORT7_TX_P
66	TX7–			—	AMC_PORT7_TX_N
67	GND	—	First	—	GND
68	RX7+	Carrier	Third	—	AMC_PORT7_RX_P
69	RX7–			—	AMC_PORT7_RX_N
70	GND	—	First	—	GND
71	SDA_L	IPMI Agent	Second	—	I2C

Table 5-25. Carrier AdvancedMC Site Pin Definitions (Side 1—Required Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
72	+12 V	—	First	—	+12 V
73	GND	—		—	GND
74	CLK1+	CLKA Driver	Third	—	AMC_CLK1_P
75	CLK1–			—	AMC_CLK1_N
76	GND	—	First	—	GND
77	CLK2+	CLKB Driver	Third	—	AMC_CLK2_P
78	CLK2–			—	AMC_CLK2_N
79	GND	—	First	—	GND
80	CLK3+	FCLK	Third	—	AMC_FCLKA_P
81	CLK3–			—	AMC_FCLKA_N
82	GND	—	First	—	GND
83	PS0#	—	Last	—	GND
84	+12 V	—	First	—	+12 V
85	GND	—		—	GND

Table 5-26. Carrier AdvancedMC Site Pin Definitions (Side 2—Optional Half)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
170	GND	—	First	—	GND
169	TDI	Carrier	Second	Carrier	JTAG
168	TDO	Module		—	JTAG
167	TRST#	Carrier	Second	Carrier	JTAG
166	TMS	Carrier	Second	Carrier	JTAG
165	TCLK	Carrier	Second	Carrier	JTAG
164	GND	—	First	—	GND
163	TX20+	Module	Third	Carrier	NC
162	TX20–			Module	NC
161	GND	—	First	—	GND
160	RX20+	Carrier	Third	Carrier	NC
159	RX20–			Module	NC
158	GND	—	First	—	GND

Table 5-26. Carrier AdvancedMC Site Pin Definitions (Side 2—Optional Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
157	TX19+	Module	Third	Carrier	NC
156	TX19–			Module	NC
155	GND	—	First	—	GND
154	RX19+	Carrier	Third	Carrier	NC
153	RX19–			Module	NC
152	GND	—	First	—	GND
151	TX18+	Module	Third	Carrier	NC
150	TX18–			Module	NC
149	GND	—	First	—	GND
148	RX18+	Carrier	Third	Carrier	NC
147	RX18–			Module	NC
146	GND	—	First	—	GND
145	TX17+	Module	Third	Carrier	NC
144	TX17–			Module	NC
143	GND	—	First	—	GND
142	RX17+	Carrier	Third	Carrier	NC
141	RX17–			Module	NC
140	GND	—	First	—	GND
139	TX16+	Module	Third	Carrier	AMC_CLK4_P
138	TX16–			Module	AMC_CLK4_N
137	GND	—	First	—	GND
136	RX16+	Carrier	Third	Carrier	AMC_CLK3_P
135	RX16–			Module	AMC_CLK3_N
134	GND	—	First	—	GND
133	TX15+	Module	Third	Carrier	NC
132	TX15–			Module	NC
131	GND	—	First	—	GND
130	RX15+	Carrier	Third	Carrier	NC
129	RX15–			Module	NC
128	GND	—	First	—	GND

Table 5-26. Carrier AdvancedMC Site Pin Definitions (Side 2—Optional Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
127	TX14+	Module	Third	Carrier	NC
126	TX14–			Module	NC
125	GND	—	First	—	GND
124	RX14+	Carrier	Third	Carrier	NC
123	RX14–			Module	NC
122	GND	—	First	—	GND
121	TX13+	Module	Third	Carrier	NC
120	TX13–			Module	NC
119	GND	—	First	—	GND
118	RX13+	Carrier	Third	Carrier	NC
117	RX13–			Module	NC
116	GND	—	First	—	GND
115	TX12+	Module	Third	Carrier	NC
114	TX12–			Module	NC
113	GND	—	First	—	GND
112	RX12+	Carrier	Third	Carrier	NC
111	RX12–			Module	NC
110	GND	—	First	—	GND
109	TX11+	Module	Third	Carrier	SRIO_SD1_TX3_P
108	TX11–			Module	SRIO_SD1_TX3_N
107	GND	—	First	—	GND
106	RX11+	Carrier	Third	Carrier	SRIO_RX3_P
105	RX11–			Module	SRIO_RX3_N
104	GND	—	First	—	GND
103	TX10+	Module	Third	Carrier	SRIO_SD1_TX2_P
102	TX10–			Module	SRIO_SD1_TX2_N
101	GND	—	First	—	GND
100	RX10+	Carrier	Third	Carrier	SRIO_RX2_P
99	RX10–			Module	SRIO_RX2_N
98	GND	—	First	—	GND

Table 5-26. Carrier AdvancedMC Site Pin Definitions (Side 2—Optional Half) (continued)

Pin #	AdvancedMC Definition		Mating	MPC8572EAMC Definition	
	Name	Driven by		Driven by	Name
97	TX9+	Module	Third	Carrier	SRIO_SD1_TX1_P
96	TX9–			Module	SRIO_SD1_TX1_N
95	GND	—	First	—	GND
94	RX9+	Carrier	Third	Carrier	SRIO_RX1_P
93	RX9–			Module	SRIO_RX1_N
92	GND	—	First	—	GND
91	TX8+	Module	Third	Carrier	SRIO_SD1_TX0_P
90	TX8–			Module	SRIO_SD1_TX0_N
89	GND	—	First	—	GND
88	RX8+	Carrier	Third	Carrier	SRIO_RX0_P
87	RX89–			Module	SRIO_RX0_N
86	GND	—	First	—	GND

5.6 MMC Control

The MMC is designed around the 32-bit MCF5213 ColdFire micro controller. This communicates with the intelligent platform management controller (IPMC) on the carrier card or µTCA Carrier Hub (MCH) in a µTCA system, over the intelligent platform management bus (IPMB), as shown in Figure 5-20.

The MMC uses the signal CF_ENABLE_PWR to control the power and reset sequence generators in the Reset CPLD. In addition the AdvancedMC has been designed so that in environments where the MMC is not present the Reset CPLD can power up the board in a in a non-MMC-enabled mode (switch selectable: SW4.4). The ColdFire supports a UART port and a background debug module (BDM) via the expansion connector.

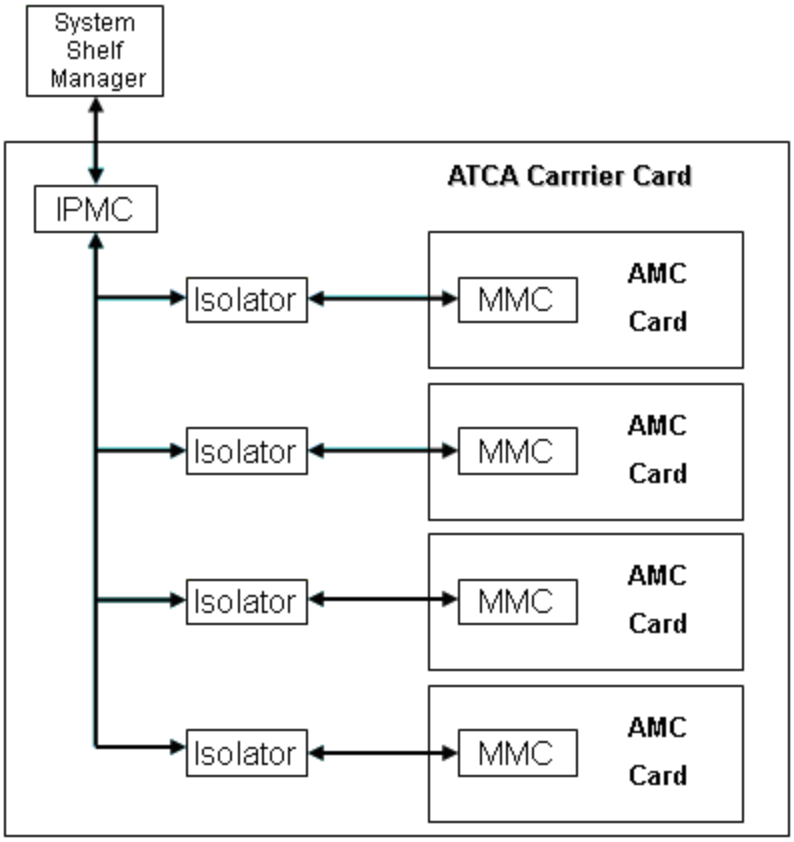

Figure 5-20. IPMC/IPMB Module Management

5.6.1 MMC Operation Overview

5.6.1.1 Module Insertion

Last mate pins PS0_N and PS1_N are used to indicate that the module is inserted. The PS1_N is pulled high by the IPMC (either by ATCA carrier or µTCA MCH). The module when fully inserted pulls PS1_N to module ground via a diode. PS1_N going low indicates the module presence to the IPMC. The IPMC senses low signal on PS1 and supplies Management Power (MP). The MP (IPMCV) is 3.3 V and cannot draw more than the AMC.0 specified 150 mA limit.

5.6.1.2 Enabling the MMC

Upon insertion, the MMC powers up and is held in a reset state until the AMC_ENABLE_N signal is pulled low. The carrier IPMC releases the module from this state by driving the AMC_ENABLE_N signal high. This is routed through the Reset CPLD to the ColdFire via the signal CF_RESET_N.

5.6.1.3 Status LEDS

Two LEDS for system status are mandated by the AMC.0 specification. These are the Blue LED and Red LED. The Red LED switches on to indicate a fault condition. The IPMC drives the state of the Blue LED during power up/hot swap operations. Figure 5-21 details the states.

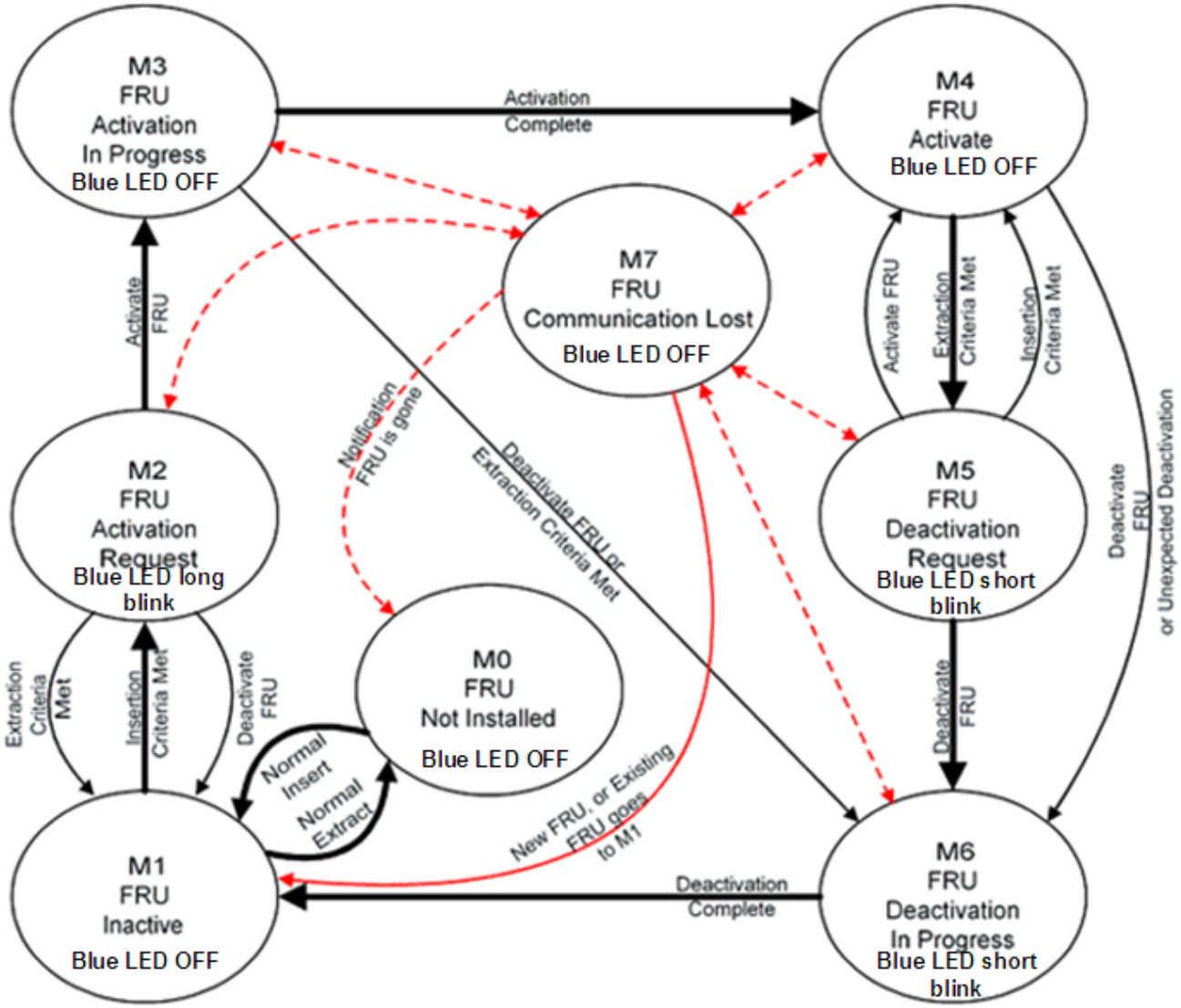

Figure 5-21. FRU State Transition Diagram

5.6.1.4 Hot Swap Switch

The Hot Swap Switch is activated by the Module latching mechanism and is used to confirm insertion or indicate a request for an extraction to the MMC. This switch signal is pulled up to Management Power so that it can be read when Payload Power is not applied. The MMC sends an event to the Carrier IPMC when the Hot Swap Switch changes state.

5.6.1.5 Module Management Communications Bus (IPMB-L)

The Out Of Band (OOB) module management may be facilitated by utilizing messages carried over IPMB-L. The IPMB-L is an I2C bus with clock line AMC_SCL and data line AMC_SDA.

5.6.1.6 Geographical Address (GA[2:0])

Three Geographic Address (AMC_GA[0:2]) pins represent the module address to the IPMC. Each GA line is in one of three states, High, Ground, or Unconnected. The MMC senses the logical states of these pins to determine its unique IPMB-L address.

5.6.1.7 Module temperature Sensors

The MMC supports two temperature sensors. The MMC monitors the temperature sensors and this data can be identified in the MMC's Sensor Data Records.

5.6.1.8 Module Voltage Sensors

Voltage sensors report the status of the power within the module. The MMC supports five power sources: 12 V, 3.3 V, 2.5 V, 1.8 V, and 1.5 V.

5.6.1.9 MMC UART

The MMC can be interrogated by the user via the ColdFire UART connector, which is located on the expansion card.

5.6.1.10 BDM Debug Header

The ColdFire device can be programmed via the BDM header, which is located on the expansion header.

5.6.1.11 Persistent Store

The module contains a serial EEPROM (SEEPROM), which can be used to store relevant data about the AdvancedMC (Serial number, etc.). Note that FRU data is stored in the ColdFire's internal memory

5.6.2 MMC User Operation

5.6.2.1 Hot Swapping

To hot swap a board complete the following steps:

Hot swapping in a board:

1. Set switch SW4.4 to ON to select the MMC present option
2. Insert the AdvancedMC into the slot with the handle extracted. The BLUE LED switches ON once it is inserted.
3. Close the handle. The BLUE LED flashes and then switches OFF. The board powers up.

Hot swapping out a board:

1. Extract the hot swap handle
2. The BLUE LED flashes and then stays ON.
3. When the BLUE LED is ON, the AdvancedMC can be removed from the chassis.

5.6.2.2 UART Terminal

The MMC output can be viewed through the UART terminal of the ColdFire (via board header J7). The UART operates at 19200-8-N-1 terminal setting. The output is displayed in Figure 5-22.

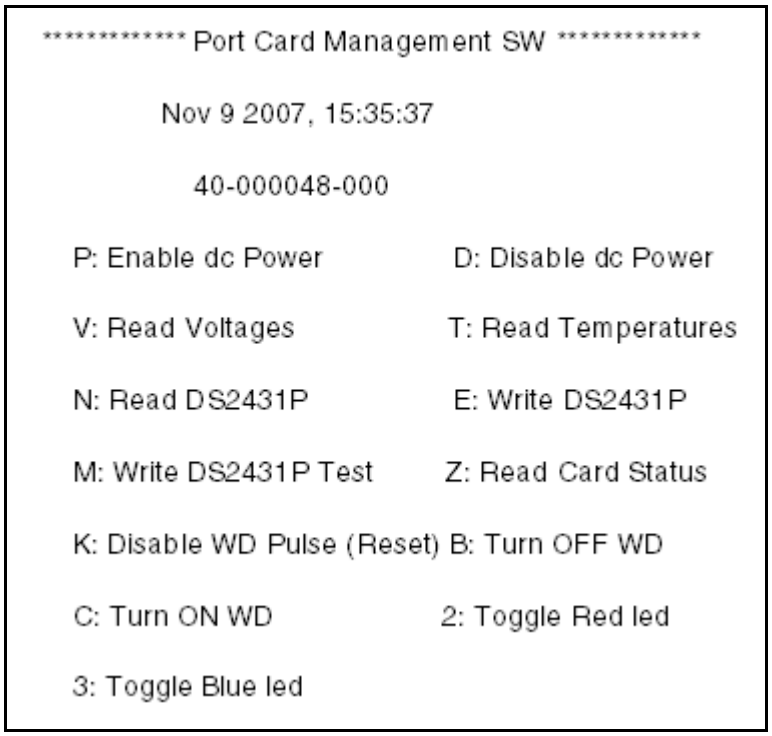

Figure 5-22. MMC UART Menu

5.6.2.3 FRU records

The MMC contains FRU information that describes the board's capabilities (e-keying and power) and inventory data. The records are described Table 5-27 through Table 5-31.

Table 5-27. FRU Common Header

Common Header			
Length	**Field**	**Value**	**Description**
1	Common Header Format Version	01	fixed value
1	Internal Use Area Starting Offset • Multiple of 8bytes, 00= not present	00	Internal Use Area not present
1	Chassis Use Area starting Offset • Multiple of 8bytes, 00= not present	00	Chassis Use Area not present

Table 5-27. FRU Common Header (continued)

Common Header			
Length	**Field**	**Value**	**Description**
1	Board Area starting Offset • Multiple of 8bytes, 00= not present	01	Board Area present, offset =8 bytes
1	Product Info Area starting Offset • Multiple of 8bytes, 00= not present	09	Product Info Area present, offset =64bytes
1	Multi-record Area starting Offset • Multiple of 8bytes, 00= not present	11	Multi-record Area present, offset =128 bytes
1	PAD –fixed to 00	00	00
1	Common header Checksum	E4	—

Table 5-28. FRU Board Information Area

Common Header			
Length	**Field**	**Value**	**Description**
1	Board Area Format version	01	Fixed
1	Board Area length	08	Length =56 Bytes
1	Language Code	19	English
3	Mfg. Date/Time Number of mins from 1/1/96—little-endian	40D562	—
1	Board Manufacturer type/length	C9	8-bit ASCII, Length= 9 Bytes
P	Board Manufacturer bytes	467265657363616c65	Freescale
1	Board Product Name type/length byte	CA	8-bit ASCII, Length= 10 Bytes
Q	Board Product Name bytes	4D504338353732414D43	MPC8572EAMC
1	Board Serial Number type/length byte	C5	8-bit ASCII, Length= 5 Bytes
N	Board Serial Number bytes	3030303030	00000
1	Board Part Number type/length byte	C9	8-bit ASCII, Length= 9 Bytes
M	Board Part Number Bytes	3730302D3233353839	700-23589
13	FRU File ID type/length/bytes	CD	File ID
R	FRU File ID Bytes	34302D 3030303034382D303031	40-000048-001
xx	Additional Custom mfg info fields	Not required	Not required
1	C1 type/length/byte encoded to indicate no more fields	C1	Fixed
Y	00—any remaining unused space	00 00 00	Fixed
1	Board area checksum	F5	Checksum

Table 5-29. FRU Product Information Area

Common Header			
Length	**Field**	**Value**	**Description**
1	Product Area Format version	01	Fixed
1	Product Area length	08	Length = 56 bytes
1	Language Code (English)	19	English
1	Manufacturer Name type/length byte	C9	8-bit ASCII, Length= 9 Bytes
N	Manufacturer Name bytes	467265657363616c65	Freescale
1	Product Name type/length byte	CA	8-bit ASCII, Length= 10 Bytes
M	Product Name bytes (MPC8572EAMC)	4D504338353732414D43	MPC8572EAMC
1	Product Part/Model Number type/length byte	CC	8-bit ASCII, Length= 12 Bytes
O	Product Part/Model Bytes	4D504338353732414D43	MPC8572EAMC
1	Product Version type/length byte (ASCII 12 bytes)	CD	8-bit ASCII, Length= 12 Bytes
R	Product Version Bytes	5265762042202850696C6F7429	Rev B (Pilot)
1	Product Serial Number type/length/bytes	C6	8-bit ASCII, Length= 6 Bytes
P	Product Serial Number (012345)	313233343536	123456
1	Asset Tag type/length byte	C0	None
Q	Asset Tag	—	—
1	FRU ID type/length byte	C0	None
R	FRU file ID bytes	—	—
xx	Custom product info area fields	—	—
1	C1h type/length byte encoded for no more fields	C1	no more fields
Y	00h any unused fields	—	Pad with 00
1	Product Info Area Checksum	DE	Checksum

Table 5-30. FRU Point-to-Point Connectivity Record

Common Header			
Length	**Field**	**Value**	**Description**
1	Record Type ID (C0)	C0	Fixed
1	End of List/version	02	Fixed
1	Record length	38	—
1	Record Checksum	AF	—

Table 5-30. FRU Point-to-Point Connectivity Record (continued)

Common Header			
Length	**Field**	**Value**	**Description**
1	Header checksum	57	—
3	Manufacturer ID	5A3100	Fixed for PICMG at 5A3100
1	PICMG record ID (19)	19	Fixed
1	Record Format version (00)	00	Fixed
1	OEM GUID Count (1 OEM GUID record defined)	1	1 record defined
16	OEM GUID List	30303030 30303030 30303030 30303030	0000000000000000
1	Record Type	80	AMC Module
1	AMC Channel Descriptor Count	04	4 Channels
3	AMC Channel Descriptor 0	FFFFE0h	Lane 0 Port Number =0, Lanes1, 2, 3 not used
3	AMC Channel Descriptor 1	FFFFE1h	Lane 0 Port Number =1, Lanes1, 2, 3 not used
3	AMC Channel Descriptor 2	F398A4h	Lanes 0,1,2,3 = Port Number 4, 5, 6, 7
3	AMC Channel Descriptor 3	F5A928h	Lanes 0,1,2,3 = Port Number 8, 9,10,11
5	**AMC Link Descriptor 0** Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00005100 00h 1h 05h 00h 00h 00b	AMC Channel ID = 0 [Breakdown below] Lane 0 Bit Flag = included Link Type = AMC.2 Ethernet — Independent Match = Exact
5	**AMC Link Descriptor 1** Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00005101 01h 1h 05h 00h 00h 00b	AMC Channel ID = 1 [Breakdown below] Lane 0 Bit Flag = included Link Type = AMC.2 Ethernet — Independent Match = Exact

Table 5-30. FRU Point-to-Point Connectivity Record (continued)

Common Header			
Length	**Field**	**Value**	**Description**
5	**AMC Link Descriptor 2** Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00006F02 02h Fh 02h 00h 00h 00b	AMC Channel ID =1 [Breakdown below] Lane 0, 1, 2, 3 Bit Flag = included Link Type = AMC.1 PCIE — Independent Match = Exact
5	**AMC Link Descriptor 3** Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00006F03 03h Fh 06h 00h 00h 00b	AMC Channel ID = 3 [Breakdown below] Lane 0, 1, 2, 3 Bit Flag = included Link Type = AMC.4 SRIO — Independent Match = Exact

Table 5-31. FRU Module Current Requirements

Common Header			
Length	**Field**	**Value**	**Description**
1	Record Type ID (C0)	C0	Fixed
1	End of List/version (last record)	82	Last Record
1	Record length	06	Length = 6 bytes
1	Record Checksum	2D	checksum
1	Header checksum	8B	checksum
3	Manufacturer ID	5A3100	Fixed for PICMG at 5A3100
1	PICMG record ID	16	Fixed
1	Record Format version (00)	00	Fixed
1	Current Draw	32	5 Amps

5.7 Thermal Requirements

A heat sink is used to cool the MPC8572E device. The heat sink definition is based on thermal simulation within an ATCA chassis with an air flow of >2 m/s. Thermal heat compound is used to ensure the heat sink makes good thermal contact with the microprocessor. Placing the MPC8572EAMC near the fan outlet also helps maximize cooling.

Appendix A
Revision History

Table A-1 provides a revision history for this document.

Table A-1. Document Revision History

Rev. Number	Date	Substantive Change(s)
1.2	11/2008	In Table 3-1, “MPC8572EAMC Memory Map,” changed 0xE8000000 to 0xF8000000 for local bus FLASH. In Table 5-4, “MPC8572E Local Bus Chip Select Resources and Memory Map,” changed 0xE8000000 to 0xF8000000 for LSC0.
1.1	09/2008	Modified note in Section 1.3.1, “External Connectors.” In Table 5-7, “MPC8572E POR Configuration DEFAULT Settings,” modified the “RapidIO Device ID” row. Modified Figure 5-8, “MPC8572E POR Configuration,” and Figure 5-19, “MPC8572EAMC, AdvancedMC Connector Signal Mapping.”
1.0	08/2008	Initial public release.