Data Sheet | May 28, 2009 | FN6359.3

Two-Phase Core Controller for AMD Mobile Turion CPUs

The ISL6264 is a two-phase buck controller with embedded gate drivers. The two-phase buck controller uses two interleaved channels to effectively double the output voltage ripple frequency and thereby reduce output voltage ripple amplitude with fewer components, lower component cost, reduced power dissipation, and smaller real estate area. ISL6264 can also be configured as single-phase controller for low power CPU applications.

The heart of the ISL6264 is the patented R^3 Technology™, Intersil's Robust Ripple Regulator modulator. Compared with the traditional multi-phase buck regulator, the R^3 Technology™ has the fastest transient response. This is due to the R^3 modulator commanding variable switching frequency during a load transient.

To boost battery life, the ISL6264 supports PSI_L for deeper sleep mode via automatically enabling different operation modes. At heavy load operation of the active mode, the regulator commands the two phase continuous conduction mode (CCM) operation. While the PSI_L is asserted during the deeper sleep mode, the ISL6264 smoothly disables one phase and operates in a one-phase diode emulation mode (DE) to maximize the efficiency at light load.

A 6-bit digital-to-analog converter (DAC) allows dynamic adjustment of the core output voltage from 0.375V to 1.55V. A 0.5% system accuracy of the core output voltage over temperature at active mode is achieved by the ISL6264.

A unity-gain differential amplifier is provided for remote CPU die sensing. This allows the voltage on the CPU die to be accurately measured and regulated per AMD mobile CPU specifications. Current sensing can be realized using either lossless inductor DCR sensing or precision resistor sensing. A single NTC thermistor network thermally compensates the gain and the time constant of the DCR variations.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6264CRZ*	ISL6264 CRZ	-10 to +100	40 Ld 6x6 QFN	L40.6x6
ISL6264CRZ-T*	ISL6264 CRZ	-10 to +100	40 Ld 6x6 QFN Tape and Reel	L40.6x6

*Please refer to TB347 for details on reel specifications.

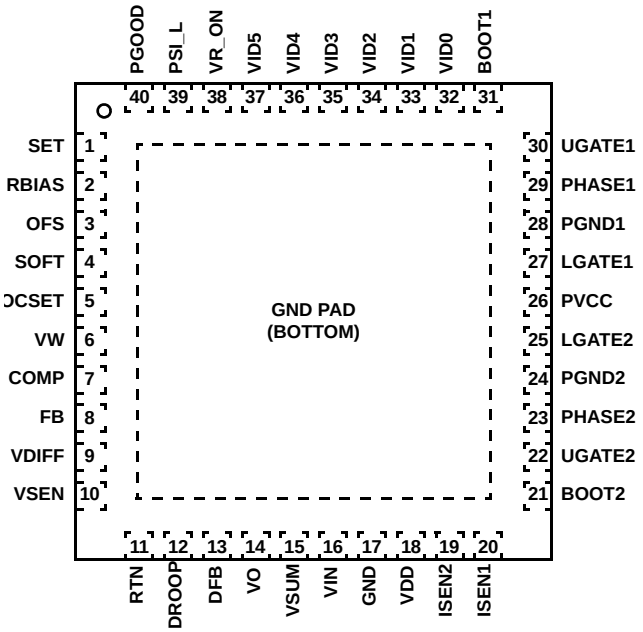
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Precision Two-phase Core Voltage Regulator
  - 0.5% System Accuracy Over-temperature
- Voltage Positioning with Adjustable Load Line and Offset
- Internal Gate Driver with 2A Driving Capability
- Dynamic Phase Adding/Dropping
- Differential Current Sensing: DCR or Resistor
- Microprocessor Voltage Identification Input
  - 6-Bit VID Input
  - 0.775V to 1.55V in 25mV Steps
  - 0.375V to 0.7625V in 12.5mV Steps
- Adjustable Reference-Voltage Offset
- Audio Filter Enable/Disable
- User Programmable Switching Frequency
- Differential Remote CPU Die Voltage Sensing
- Static and Dynamic Current Sharing
- Overvoltage, Undervoltage, and Overcurrent Protection
- Pb-Free (RoHS Compliant)

Pinout

ISL6264
(40 LD QFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3 - +7V
Battery Voltage, VIN. . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE). . . . . -0.3V to +7V(DC)
. . . . . -0.3V to +9V (<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE -0.3V (DC) to BOOT
PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE) . . . . . -0.3V (DC) to VDD+0.3V
-2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
ALL Other Pins. . . . . -0.3V to (VDD + 0.3V)
Open Drain Outputs, PGOOD . . . . . -0.3 - +7V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package.	32	4

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Voltage, VIN. . . . . +5V to 25V
Ambient Temperature . . . . . -10°C to +100°C
Junction Temperature . . . . . -10°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

VDD = 5V, T_A = -10°C to +100°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT POWER SUPPLY						
I_{VDD}	+5V Supply Current	VR_ON = 3.3V	-	3.1	3.6	mA
		VR_ON = 0V	-	-	1	µA
I_{VIN}	Battery Supply Current at VIN Pin	VR_ON = 0V, VIN = 25V	-	-	1	µA
POR_r	POR (Power-On Reset) Threshold	VDD Rising	-	4.35	4.5	V
POR_f		VDD Falling	3.9	4.1	-	V
SYSTEM AND REFERENCES						
%Error (V_{DD_core})	System Accuracy	No load, closed loop, active mode, T_A = +25°C to +100°C, VID = 0.75V to 1.55V	-0.5	-	0.5	%
		VID = 0.425V to 0.75V	-2	-	+2	%
		VID = 0.375V to 0.425V	-4	-	+4	%
R_{RBIAS}	RBIAS Voltage	R_{RBIAS} = 147kΩ	1.5	1.52	1.54	V
V_{DD_core} (max)	Maximum Output Voltage	VID = [000000]	-	1.55	-	V
V_{DD_core} (min)	Minimum Output Voltage	VID = [111111]	-	0.375	-	V
CHANNEL FREQUENCY						
f_{SW}	Nominal Channel Frequency	R_{FSET} = 6.81kΩ, 2 Channel operation, V_{COMP} = 2V	285	300	315	kHz
	Adjustment Range		200	-	500	kHz
AMPLIFIERS						
	Droop Amplifier Offset		-0.3	-	0.3	mV
A_{V0}	Error Amp DC Gain (Note 3)		-	90	-	dB
GBW	Error Amp Gain-Bandwidth Product (Note 3)	C_L = 20pF	-	18	-	MHz
SR	Error Amp Slew Rate (Note 3)	C_L = 20pF	-	5.0	-	V/µs

Electrical Specifications VDD = 5V, T_A = -10°C to +100°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISEN1, ISEN2						
	Imbalance Voltage		-	-	1	mV
	Input Bias Current		-	20	-	nA
SOFT START CURRENT						
I_{SS}	Soft Start Current		-48	-43	-38	µA
I_2	Soft Current during VID on the Fly		±185	±210	±235	µA
GATE DRIVER DRIVING CAPABILITY						
$R_{SRC(UGATE)}$	UGATE Source Resistance (Note 4)	500mA Source Current	-	1	1.5	Ω
$I_{SRC(UGATE)}$	UGATE Source Current (Note 4)	V_{UGATE_PHASE} = 2.5V	-	2	-	A
$R_{SNK(UGATE)}$	UGATE Sink Resistance (Note 4)	500mA Sink Current	-	1	1.5	Ω
$I_{SNK(UGATE)}$	UGATE Sink Current ((Note 4)	V_{UGATE_PHASE} = 2.5V	-	2	-	A
$R_{SRC(LGATE)}$	LGATE Source Resistance (Note 4)	500mA Source Current	-	1	1.5	Ω
$I_{SRC(LGATE)}$	LGATE Source Current (Note 4)	V_{LGATE} = 2.5V	-	2	-	A
$R_{SNK(LGATE)}$	LGATE Sink Resistance (Note 4)	500mA Sink Current	-	0.5	0.9	Ω
$I_{SNK(LGATE)}$	LGATE Sink Current(Note 4)	V_{LGATE} = 2.5V	-	4	-	A
$R_{p(UGATE)}$	UGATE to PHASE Resistance		-	1	-	kΩ
GATE DRIVER SWITCHING TIMING (Refer to"ISL6264 Gate Driver Timing Diagram" on page 4)						
t_{RU}	UGATE Rise Time (Note 3)	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
t_{RL}	LGATE Rise Time (Note 3)	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
t_{FU}	UGATE Fall Time (Note 3)	PV_{CC} = 5V, 3nF Load	-	8.0	-	ns
t_{FL}	LGATE Fall Time (Note 3)	PV_{CC} = 5V, 3nF Load	-	4.0	-	ns
t_{PDHU}	UGATE Turn-on Propagation Delay	PV_{CC} = 5V, Outputs Unloaded	23	30	44	ns
t_{PDHL}	LGATE Turn-on Propagation Delay	PV_{CC} = 5V, Outputs Unloaded	7	15	30	ns
BOOTSTRAP DIODE						
	Forward Voltage	V_{DDP} = 5V, Forward Bias Current = 2mA	0.43	0.58	0.67	V
	Leakage	V_R = 16V	-	-	1	µA
POWER GOOD and PROTECTION MONITOR						
V_{OL}	PGOOD Low Voltage	I_{PGOOD} = 4mA	-	0.11	0.4	V
I_{OH}	PGOOD Leakage Current	P_{GOOD} = 3.3V	-1	-	1	µA
tpgd	PGOOD Delay	VR_ON Enable to PGOOD High when C_{SOFT} = 47nF	6.3	7.6	8.9	ms
O_{VH}	Overvoltage Threshold	V_O rising above setpoint >1ms	155	195	235	mV
O_{VHS}	Severe Overvoltage Threshold	V_O rising above setpoint >0.5µs	1.775	1.8	1.825	V
	OCSET Reference Current	Rbias = 147kΩ	10	10.2	10.4	µA
	OC Threshold Offset	DROOP rising above OCSET >120µs	-3	-	3	mV
	Current Imbalance Threshold	Difference between ISEN1-ISEN2 >1ms	-	8	-	mV
UV_f	Undervoltage Threshold (VDIFF-SOFT)	V_O falling below setpoint for >1ms	-300	-250	-200	mV

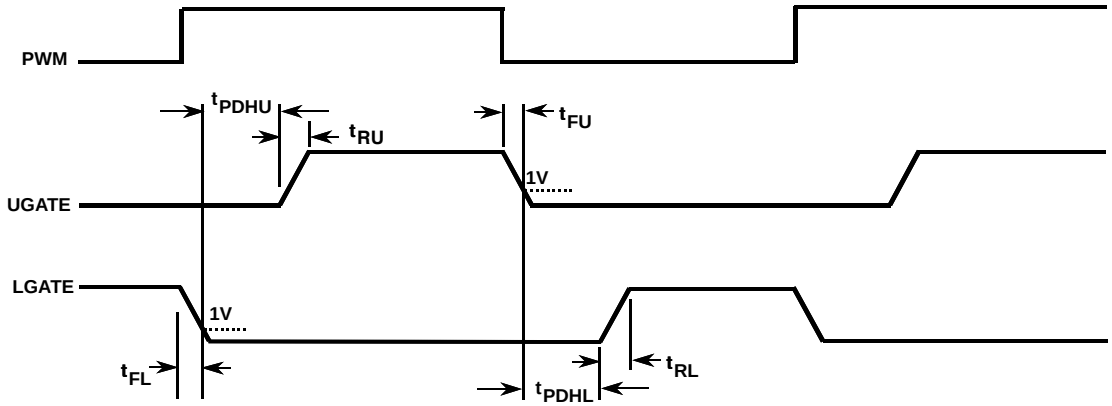
Electrical Specifications VDD = 5V, T_A = -10°C to +100°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFFSET FUNCTION						
I_{OFFSET}	OFS Pin Current	36.5kΩ resistor connects OFS pin to GND.	-	33	-	µA
I_{FB}	FB Pin Souring Current		-	33	-	µA
LOGIC INPUTS						
$V_{IL(3.3V)}$	VR_ON		-	-	1	V
$V_{IH(3.3V)}$	VR_ON		2.3	-	-	V
$I_{IL(3.3V)}$	Leakage current of VR_ON	Logic input is low	-1	0	-	µA
$I_{IL(3.3V)}$		Logic input is high at 3.3V	-	0	1	µA
$V_{IL(3.3V)}$	SET		-	-	1	V
$V_{IH(3.3V)}$	SET		2.3	-	-	V
$I_{IL(3.3V)}$	Leakage Current of SET	Logic input is low	-1	0	-	µA
$I_{IL(3.3V)}$		Logic input is high at 3.3V	-	0.45	1	µA
$V_{IL(1.0V)}$	DAC(VID0 - VID5) and PSI_L Input Low		-	-	0.3	V
$V_{IH(1.0V)}$	DAC(VID0 - VID5), PSI_L input High		0.7	-	-	V
$I_{IL(1V)}$	Leakage Current of DAC (VID0 - VID5) and PSI_L	Logic input is low	-1	0	-	µA
		Logic input is high at 1V	-	0.45	1	µA

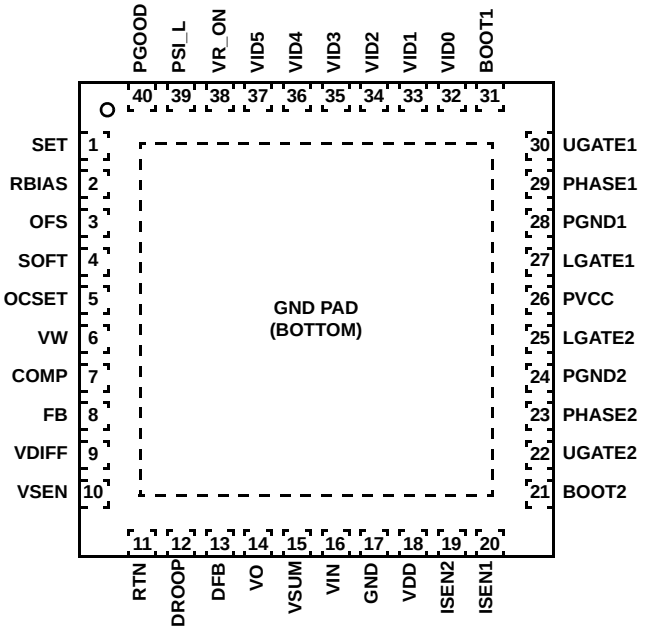
NOTES:

3. Limits should be considered typical and are not production tested.
4. Limits established by characterization and are not production tested.

ISL6264 Gate Driver Timing Diagram



Functional Pin Description



SET

Logic low enables the audio filter which only allows above 20kHz operation. Logic high disables the audio filter.

RBIAS

147kΩ resistor to GND sets internal current reference, ~10µA, for the overcurrent protection setting.

OFS

A resistor from this pin to GND programs a DC current source for generating a positive offset voltage across the resistor between FB and VDIFF pins. The OFS pin voltage is 1.2V.

SOFT

A capacitor from this pin to GND pin sets the maximum slew rate of the output voltage. The SOFT pin is the non-inverting input of the error amplifier. A 210µA internal current source is generated to charge or discharge the SOFT pin capacitor to determine the slew-rate of VID. During the start-up process, the current source is reduced to 43µA.

OCSET

Overcurrent protection set input. A resistor from this pin to VO sets DROOP voltage limit for OC trip. A 10µA current source is connected internally to this pin.

VW

A resistor from this pin to COMP programs the switching frequency (for example, 6.81k ~ 300kHz).

COMP

This pin is the output of the error amplifier.

FB

This pin is the inverting input of the error amplifier.

VDIFF

This pin is the output of the differential amplifier.

VSEN

Remote core voltage sense input.

RTN

Remote core voltage sense return.

DROOP

Output of the droop amplifier. The voltage level at this pin is the sum of Vo and the programmed droop voltage by the external resistors.

DFB

This pin is the inverting input of the droop amplifier.

VO

An input to IC reporting the local output voltage.

VSUM

This pin is connected to the summation junction of channel current sensing.

VIN

It is used for input voltage feed forward to improve input line transient performance.

GND

Signal ground. Connect to local controller ground.

VCC

5V bias power supply for the ISL6264 controller.

ISEN2

Individual current sharing sensing for channel 2.

ISEN1

Individual current sharing sensing for channel 1.

BOOT2

This pin is the upper gate driver supply voltage for phase 2. An internal boot strap diode is connected to the PVCC pin.

UGATE2

Upper MOSFET gate signal for phase 2.

PHASE2

The phase node of phase 2. This pin should connect to the source of upper MOSFET. It is the return path for the upper MOSFET drive.

PGND2

The return path of the lower gate driver for phase 2.

LGATE2

Lower-side MOSFET gate signal for phase 2.

PVCC

5V power supply for gate drivers.

LGATE1

Lower-side MOSFET gate signal for phase 1.

PGND1

The return path of the lower gate driver for phase 1.

PHASE1

The phase node of phase 1. This pin should connect to the source of upper MOSFET. It is the return path for the upper MOSFET drive.

UGATE1

Upper MOSFET gate signal for phase 1.

BOOT1

This pin is the upper gate driver supply voltage for phase 1. An internal boot strap diode is connected to the PVCC pin.

VID0, VID1, VID2, VID3, VID4, VID5

VID input with VID0 is the least significant bit (LSB) and VID5 is the most significant bit (MSB).

VR_ON

A high level logic signal on this pin enables the ISL6264.

PSI_L

Sleeper mode indicator. When asserted low, ISL6264 initiates the single-phase operation.

PGOOD

Power good open-drain output. Will be pulled up externally by a resistor to V_{CCP} or 3.3V.

Function Block Diagram

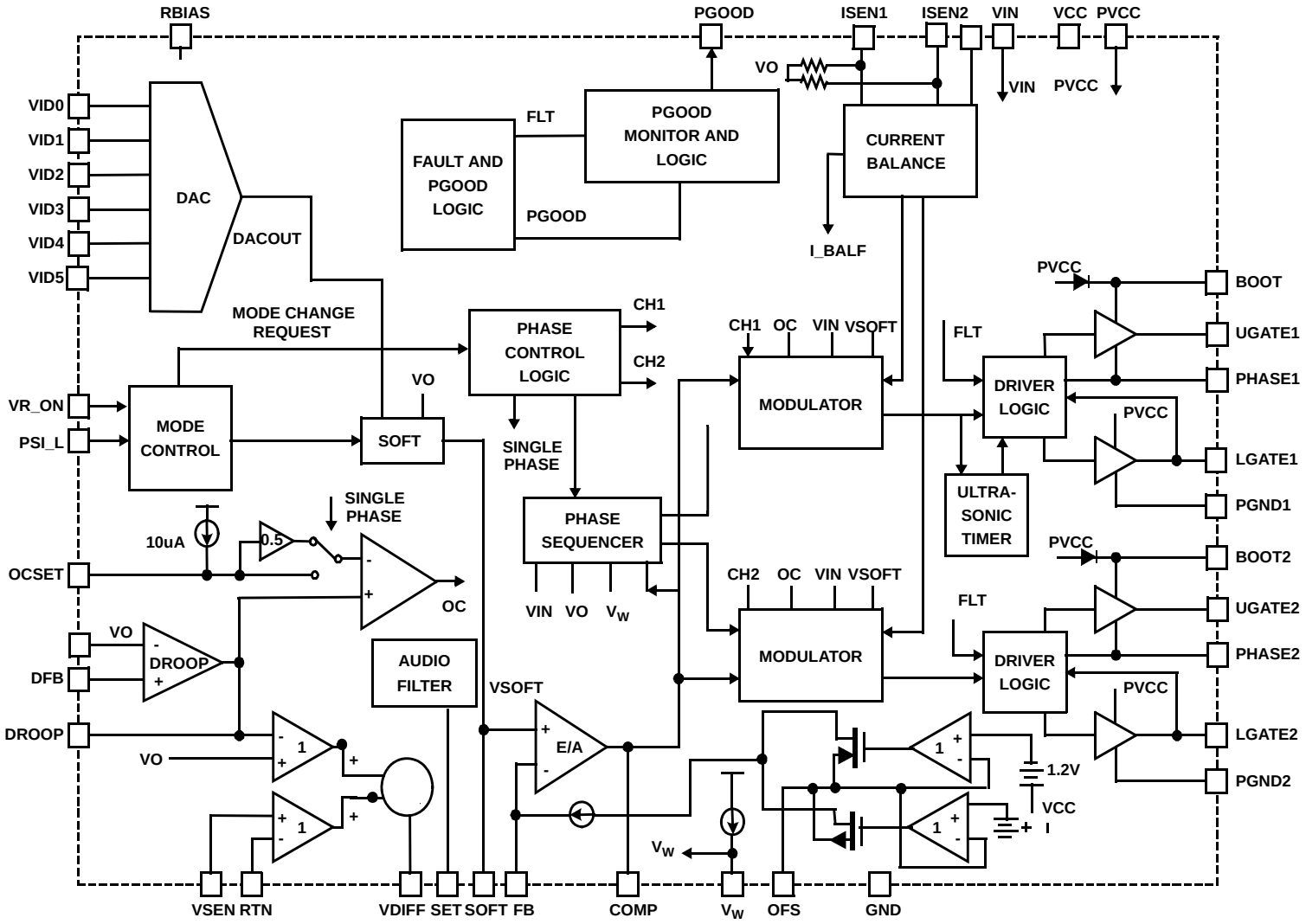


FIGURE 1. SIMPLIFIED FUNCTION BLOCK DIAGRAM OF ISL6264

Simplified Application Circuit for DCR Current Sensing

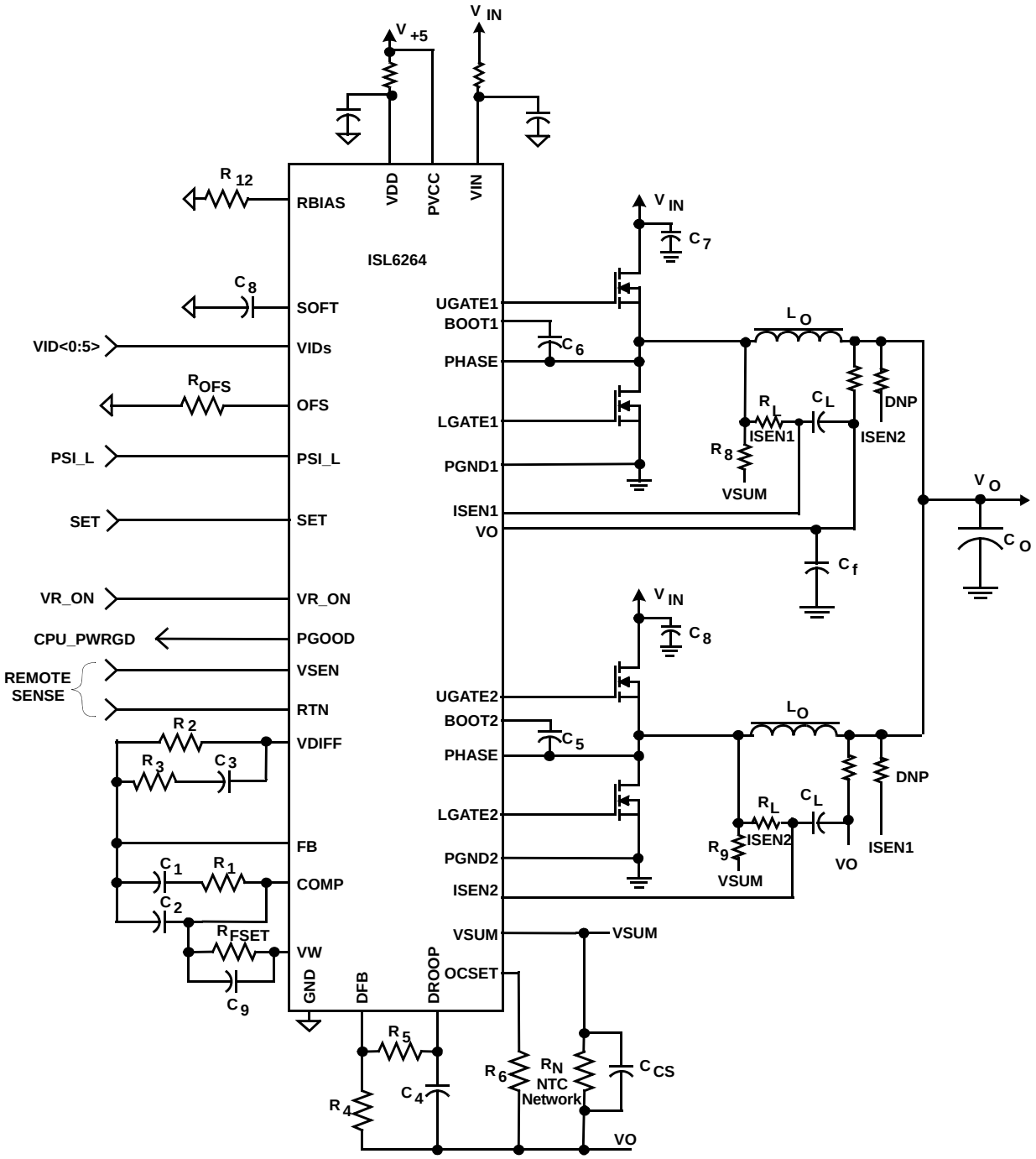


FIGURE 2. ISL6264 BASED TWO-PHASE BUCK CONVERTER WITH INDUCTOR DCR CURRENT SENSING

Simplified Application Circuit for Resistor Current Sensing

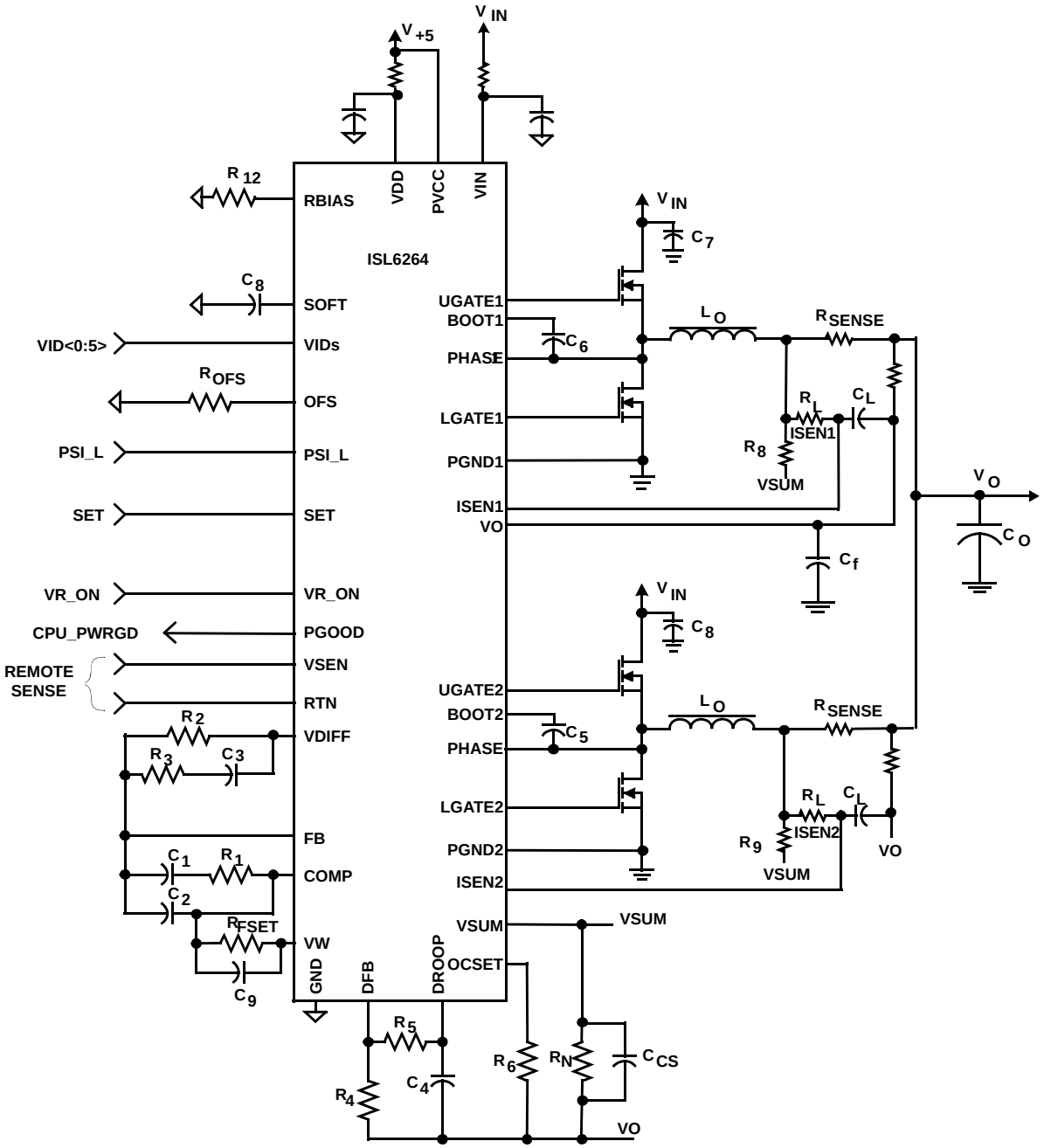


FIGURE 3. ISL6264 BASED TWO-PHASE BUCK CONVERTER WITH RESISTOR CURRENT SENSING

Typical Performance Curves (0.36µH filter inductor, 4x330µF output SP caps and 32x22µF ceramic caps)

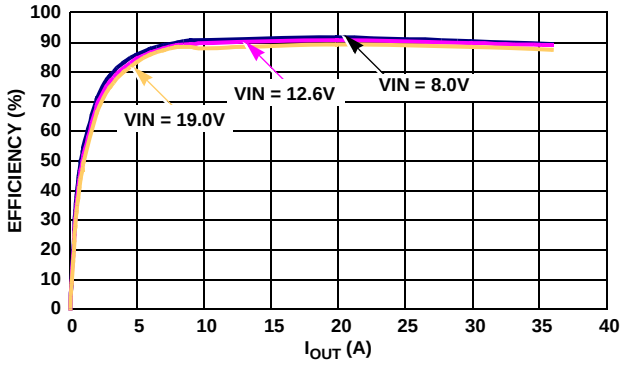


FIGURE 4. ACTIVE MODE EFFICIENCY, 2 PHASE, CCM, PSI_l = HIGH, VID = 1.15V

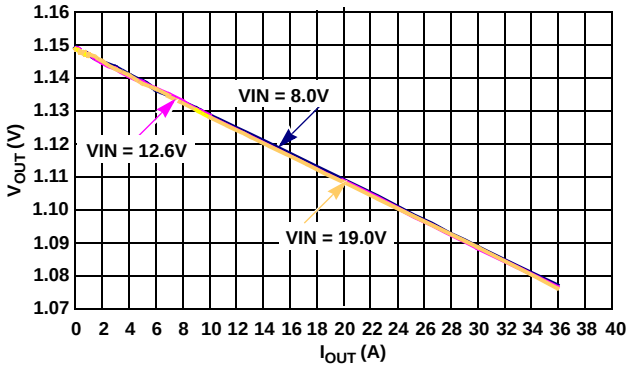


FIGURE 5. ACTIVE MODE LOAD LINE, 2 PHASE, CCM, PSI_L = HIGH, VID = 1.15V

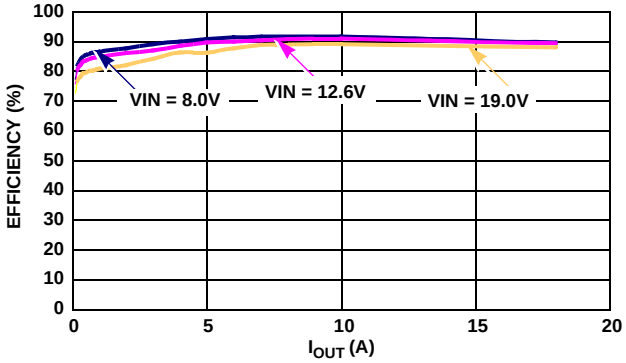


FIGURE 6. ACTIVE MODE EFFCIENCY, 1 PHASE, DE, PSI_L = LOW, V_{ID} = 1.15V

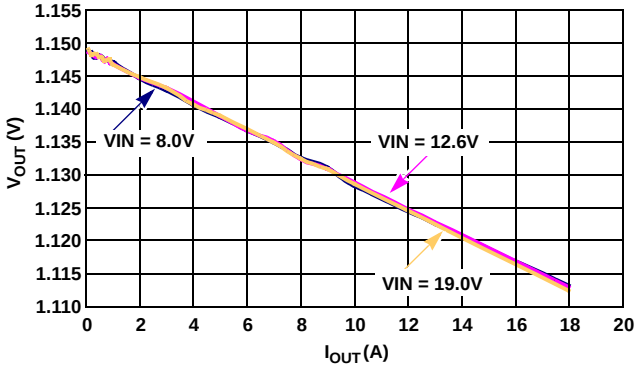


FIGURE 7. ACTIVE MODE LOAD LINE, 1 PHASE, DE, PSI_L = LOW, VID = 1.15V

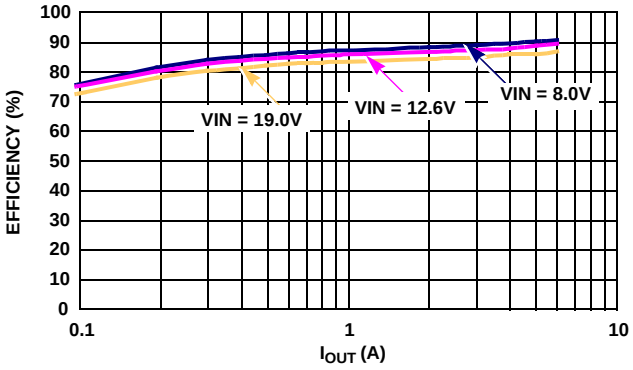


FIGURE 8. EFFICIENCY OF 1-PHASE DE MODE, PSI_l = LOW. DCM MODE, VID = 0.9V, OFFSET = 33mV

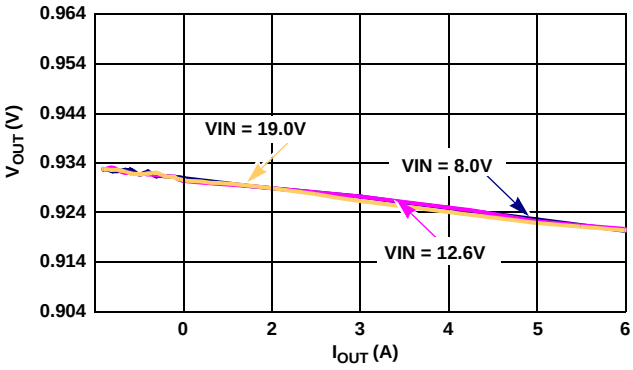


FIGURE 9. 1-PHASE DE MODE LOAD LINE, PSI_l = LOW, VID = 0.9V, OFFSET = 33mV

Typical Performance Curves (0.36µH filter inductor, 4x330µF output SP caps and 32x22µF ceramic caps) **(Continued)**

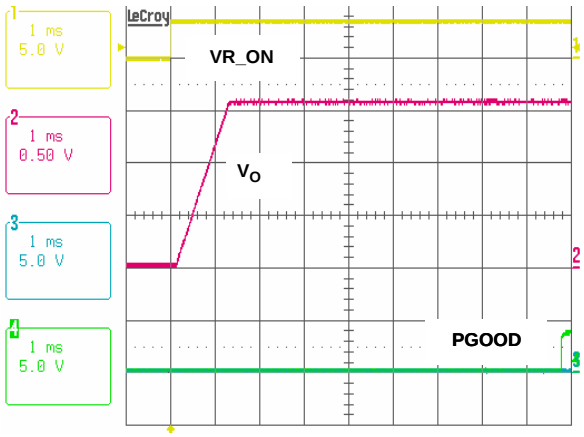


FIGURE 10. SOFT START WAVEFORM AT VID = 1.55V, ILOAD = 0A

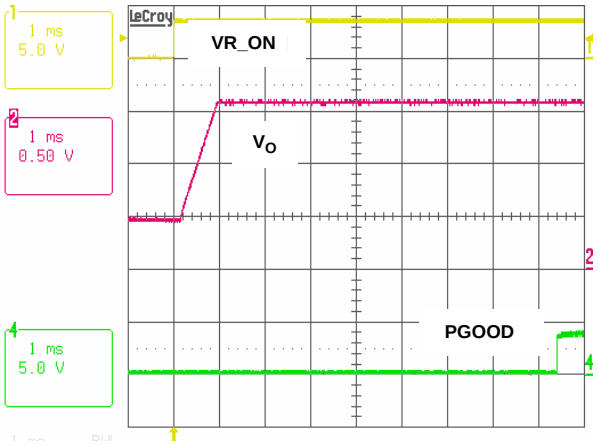


FIGURE 11. PRE-BIASED VO SOFT START AT VID = 1.55V, ILOAD = 0A

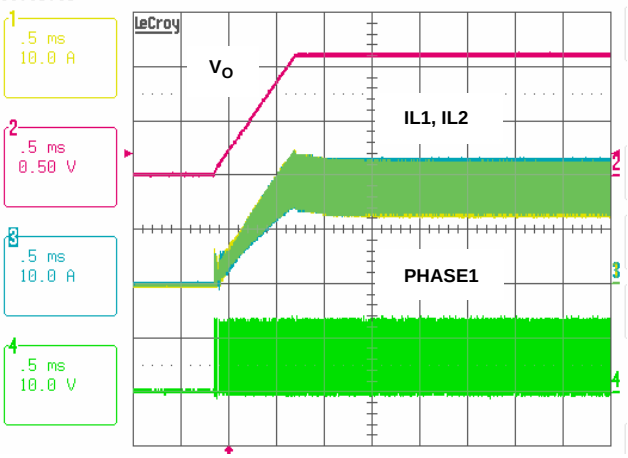


FIGURE 12. SOFT START WAVEFORM SHOWING CURRENT SHARING AT VIN = 12.6V, VID = 1.2V AND ILOAD = 36A

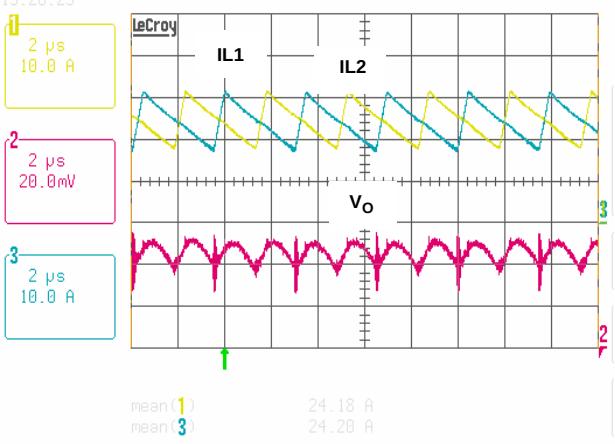


FIGURE 13. PHASE CURRENT BALANCE, ILOAD = 36A AND VID = 1.55V

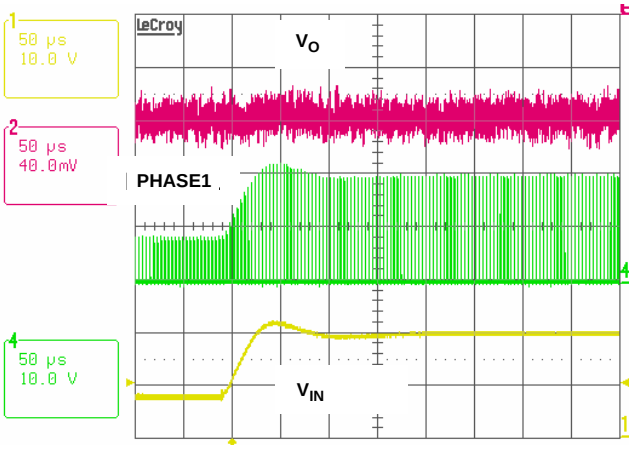


FIGURE 14. 8V TO19V INPUT LINE TRANSIENT RESPONSE AT ILOAD = 5A AND VID = 1.15V

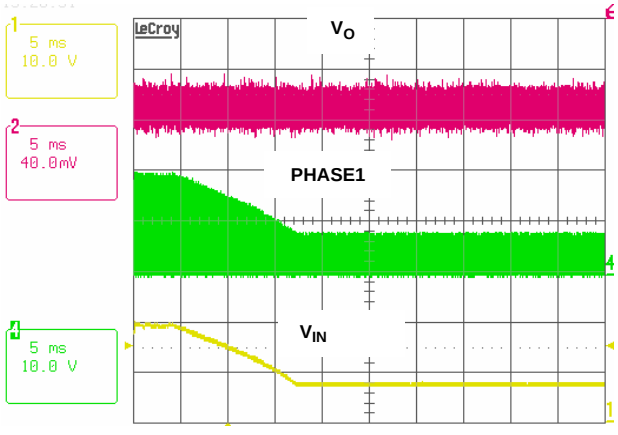


FIGURE 15. 19V TO >8V INPUT LINE TRANSIENT RESPONSE AT ILOAD = 5A AND VID = 1.15V

Typical Performance Curves (0.36µH filter inductor, 4x330µF output SP caps and 32x22µF ceramic caps) **(Continued)**

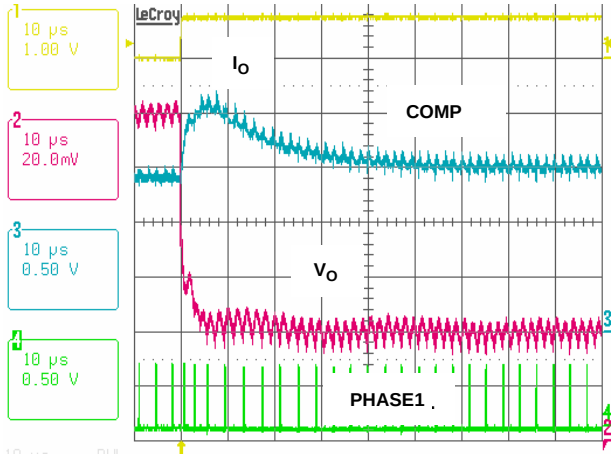


FIGURE 16. LOAD APPLICATION RESPONSE AT 2-PHASE CCM, VIN = 19V, ILOAD = 10A→46A, AND VID = 1.15V

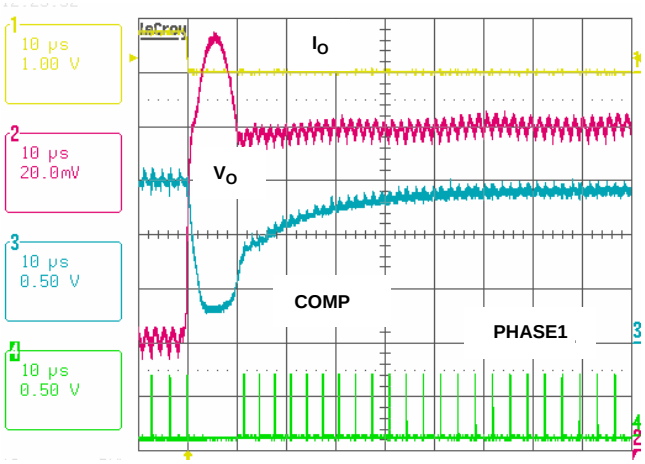


FIGURE 17. LOAD RELEASE RESPONSE AT 2-PHASE CCM, VIN = 19V, ILOAD = 46A→10A, AND VID = 1.15V

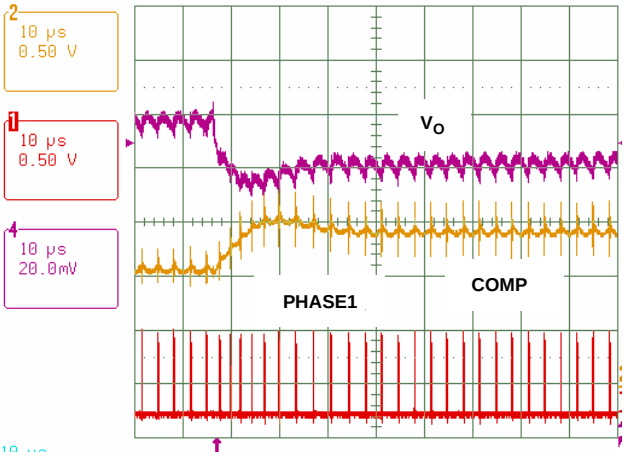


FIGURE 18. LOAD APPLICATION RESPONSE AT 1-PHASE DE MODE, ILOAD = 4A→19A, PSI_L = 0, AND VID = 1V

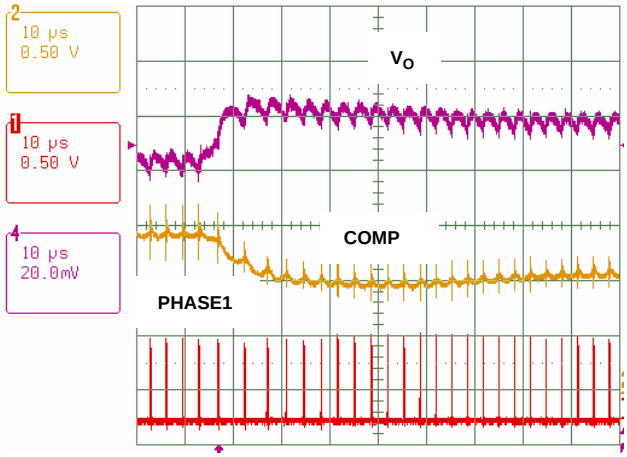


FIGURE 19. LOAD RELEASE RESPONSE AT 1-PHASE DE MODE, ILOAD = 19A→4A, PSI_L = 0, AND VID = 1V

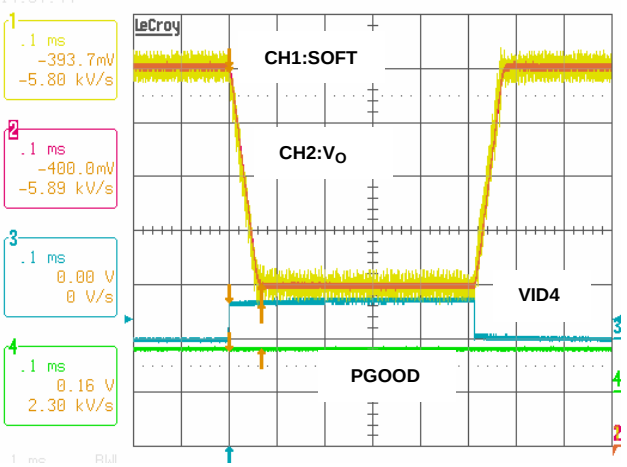


FIGURE 20. VID TRANSITION RESPONSE AT 2-PHASE CCM MODE, VIN = 12.6V AND VID = 1.55V←→ 1.15V

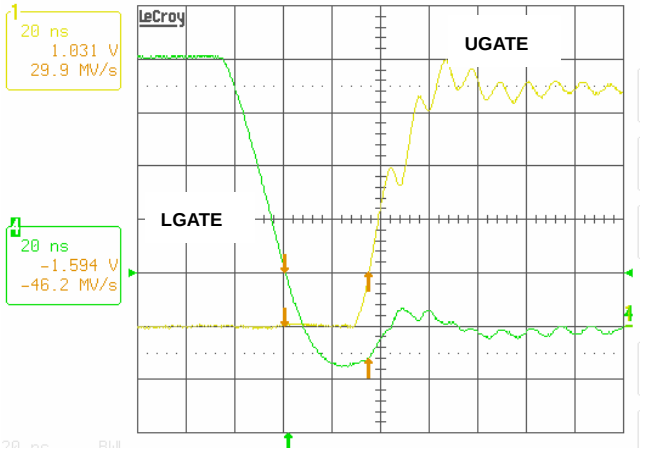


FIGURE 21. GATE DRIVER WAVEFORMS AT VIN = 8V, ILOAD = 40A, 2-PHASE MODE. 2 X IRF7821 AS UPPER DEVICE AND 2 X IRF7832 AS LOWER DEVICE

Typical Performance Curves (0.36µH filter inductor, 4x330µF output SP caps and 32x22µF ceramic caps) **(Continued)**

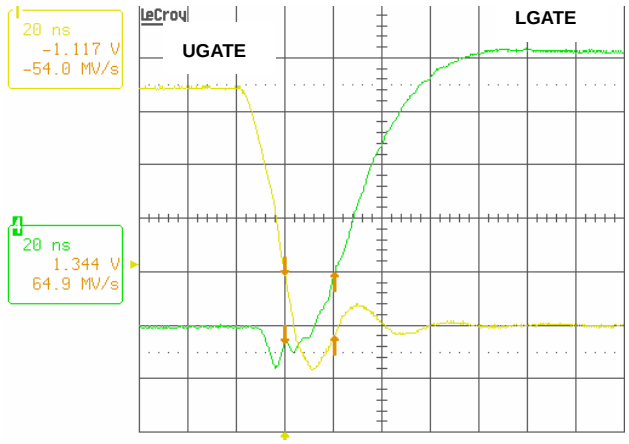


FIGURE 22. GATE DRIVER WAVEFORMS AT VIN = 8V, ILOAD = 40A, 2 X IRF7821 AS UPPER MOSFET AND 2 X IRF7832 AS LOWER MOSFET

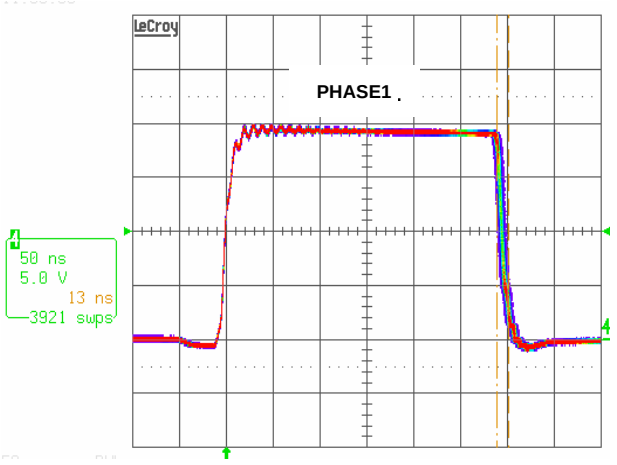


FIGURE 23. PHASE NODE JITTER PERFORMANCE AT VIN = 19V, ILOAD = 40A AND VID = 1.55V

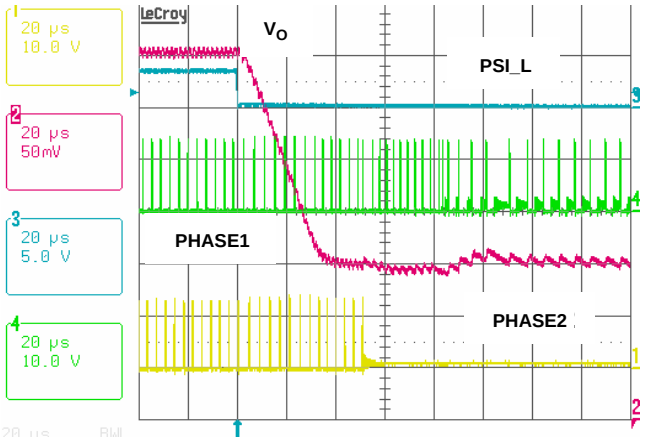


FIGURE 24. DEEPER SLEEP MODE ENTRY WITH PSI_L TOGGLING FROM HIGH TO LOW AND VID FROM 1.15V TO 0.95V

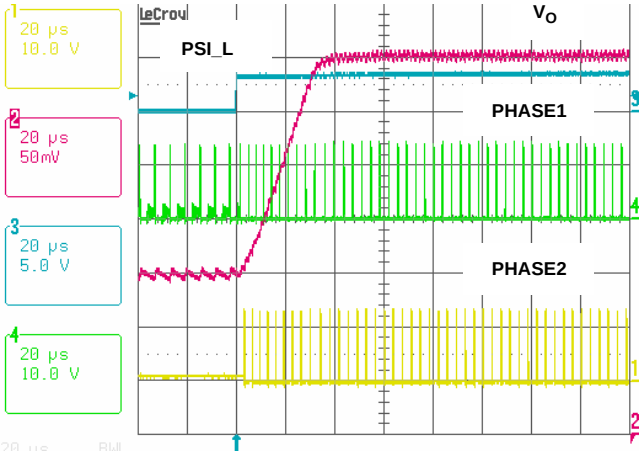


FIGURE 25. DEEPER SLEEP MODE EXIT WITH PSI_L TOGGLING FROM LOW TO HIGH AND VID FROM 0.95V TO 1.15V

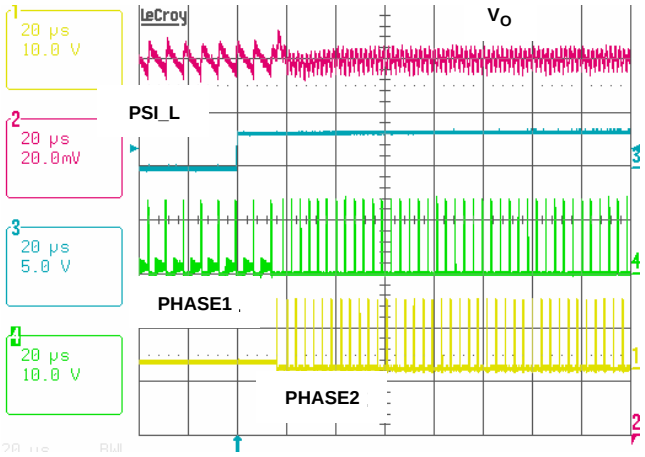


FIGURE 26. TRANSITION FROM 1-DE TO 2-CCM VIA PSI_L TOGGLING FROM LOW TO HIGH AND ILOAD = 2A

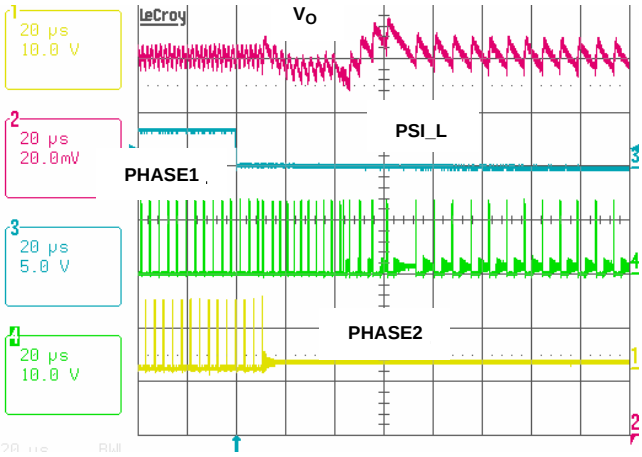


FIGURE 27. TRANSITION FROM 2-CCM TO 1-DE VIA PSI_L TOGGLING FROM HIGH TO LOW AND ILOAD = 2A

Theory of Operation

The ISL6264 is a two-phase regulator providing the power to AMD Mobile CPUs such as the Turion processor and includes integrated gate drivers for reduced system cost and board area. The regulator provides optimum steady-state and transient performance for microprocessor core applications up to 50A. System efficiency is enhanced by idling a phase at low-current and implementing automatic DCM-mode operation when PSI_L is asserted to logic low.

The heart of the ISL6264 is the R^3 Technology™, Intersil's Robust Ripple Regulator modulator. The R^3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. The ISL6264 modulator internally synthesizes an analog of the inductor ripple current and uses hysteretic comparators on those signals to establish PWM pulse widths. Operating on these large-amplitude, noise-free synthesized signals allows the ISL6264 to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic controllers, the ISL6264 has an error amplifier that allows the controller to maintain a 0.5% voltage regulation accuracy throughout the VID range from 0.75V to 1.55V.

The hysteresis window voltage is relative to the error amplifier output such that load current transients results in increased switching frequency, which gives the R3 regulator a faster response than conventional fixed frequency PWM controllers. Transient load current is inherently shared between active phases due to the use of a common hysteretic window voltage. Individual average phase voltages are monitored and controlled to equally share the static current among the active phases.

Start-up Timing

With the controller's +5V VDD voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic HIGH threshold. Approximately 100ms later, SOFT and V_{OUT} begin ramping toward the final VID voltage. At startup, the regulator always operates in a 2-phase CCM mode, regardless of PSI_L control signal assertion levels. During this interval, the SOFT cap is charged by a 43µA current source. If the SOFT capacitor is selected to be 47nF, the SOFT ramp will be at 0.9mV/s slew rate. Once V_{OUT} is within 10% of the VID voltage, approximately 7ms later, PGOOD is asserted HIGH. Typical start-up timing is shown in Figure 28. The SOFT cap is charged/discharged by approximate 200µA after the start-up. Therefore, V_{OUT} slews at about 4mV/s to the voltage set by the VID pins.

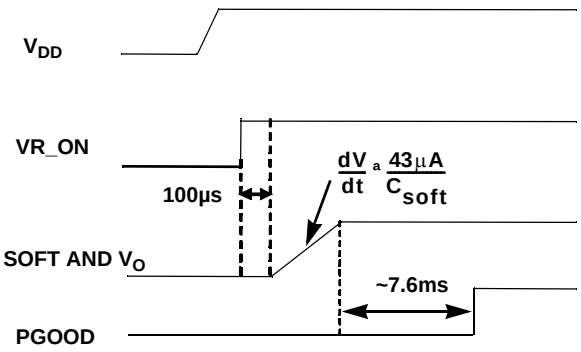


FIGURE 28. SOFT START WAVEFORMS

Static Operation

After the start sequence, the output voltage will be regulated to the value set by the VID inputs per Table 1. The entire VID table is presented in the AMD specification. The ISL6264 will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V.

TABLE 1. V_{ID} TABLE FOR AMD 6-BIT V_{ID} CPU

VID5	VID4	VID3	VID2	VID1	VID0	VOUT (V)
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000

TABLE 1. V_{ID} TABLE FOR AMD 6-BIT V_{ID} CPU (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VOUT (V)
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

A fully-differential amplifier implements core voltage sensing for precise voltage control at the microprocessor die. The inputs to the amplifier are the VSEN and RTN pins.

As the load current increases from zero, the output voltage will droop from the VID table (Table 1) value by an amount proportional to current to achieve the proper load line. The ISL6264 provides for current to be measured using either resistors in series with the channel inductors as shown in the application circuit of Figure 3, or using the intrinsic series resistance of the inductors as shown in the application circuit of Figure 2. In both cases signals representing the inductor currents are summed at VSUM, which is the non-inverting input to the DROOP amplifier shown in the block diagram of Figure 1. The voltage at the DROOP pin minus the output voltage, VO, is a high-bandwidth analog of the total inductor current. This voltage is used as an input to a differential amplifier to achieve the load line, and also as the input to the overcurrent protection circuit.

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus maintaining the load-line accuracy.

In addition to monitoring the total current (used for DROOP and overcurrent protection), the individual channel average currents are also monitored and used for balancing the load between channels. The IBAL circuit will adjust the channel pulse-widths up or down relative to the other channel to cause the voltages presented at the ISEN pins to be equal.

The ISL6264 controller can be configured for two-channel operation, with the channels operating 180° apart. The channel PWM frequency is determined by the value of RFSET connected to pin VW as shown in Figure 2 and Figure 3. Input and output ripple frequencies will be the channel PWM frequency multiplied by the number of active channels.

High Efficiency Operation Mode

The ISL6264 has two operating modes to optimize efficiency. The controller's operational modes are designed to work in conjunction with the PSI_L control signal to maintain the optimal system configuration. These operating modes are established as shown in Table 2. At high current levels, the system will operate with both phases fully active, responding rapidly to transients and deliver the maximum power to the load. At reduced load current levels, one of the phases may be idled. This configuration will minimize switching losses, while still maintaining transient response capability. At the lowest current levels, the controller automatically configures the system to operate in single-phase automatic-DCM mode, thus achieving the highest possible efficiency. In this mode of operation, the lower FET will be configured to automatically detect and prevent discharge current flowing from the output capacitor through the inductors, and the switching frequency will be proportionately reduced, thus greatly reducing both conduction and switching losses.

TABLE 2.

	PSI_L = LOGIC HIGH	PSI_L = LOGIC LOW
Operation	2-CCM	1-DE (diode emulation)

Smooth mode transitions are facilitated by the R3 Technology™, which correctly maintains the internally synthesized ripple currents throughout mode transitions. The regulator is thus able to deliver the appropriate current to the load throughout mode transitions. The controller contains embedded mode-transition algorithms which robustly maintain voltage-regulation for all control signal input sequences and durations.

Mode-transition sequences will often occur in concert with VID changes; therefore the timing of the mode transition of ISL6264 has been carefully designed to work in concert with VID changes. For example, transitions into single-phase mode if PSI_L and VID toggles at the same time will be delayed until the VID induced voltage ramp is complete, to allow the associated output capacitor charging current is shared by both inductor paths. While in single-phase automatic-DCM mode with PSI_L = logic low, VID changes will initiate an immediate return to two-phase CCM mode during the VID transition. This ensures that both inductor paths share the output capacitor charging current and are fully active for the subsequent load current increases.

The controller contains internal counters which prevent spurious control signal glitches from resulting in unwanted mode transitions. Control signals of less than two switching periods do not result in phase-idling. Signals of less than seven switching periods do not result in implementation of automatic-DCM mode.

While transitioning to single-phase operation, the controller smoothly transitions current from the idling-phase to the active-phase, and detects the idling-phase zero-current condition. During transitions into automatic-DCM or forced-CCM mode, the timing is carefully adjusted to eliminate output voltage excursions. When a phase is added, the current balance between phases is quickly restored.

Dynamic Operation

The ISL6264 responds to changes in VID command voltage by slewing to new voltages with a dV/dt set by the SOFT capacitor. The internal current source of 230µA is used to charge or discharge the SOFT capacitor.

Intersil's R^3 Technology™ has intrinsic voltage feed forward. As a result, high-speed input voltage steps do not result in significant output voltage perturbations. In response to load current step increases, the ISL6264 will transiently raise the switching frequency so that response time is decreased and current is shared by two channels.

Protection

The ISL6264 provides overcurrent, overvoltage, and undervoltage protection as shown in Table 3.

Overcurrent protection is tied to the voltage droop which is determined by the resistors selected as described in the "Component Selection and Application" section on page 17. After the load-line is set, the OCSET resistor can be selected to detect overcurrent at any level of droop voltage. An overcurrent fault will occur when the load current exceeds the overcurrent setpoint voltage while the regulator is in a 2-phase mode. While the regulator is in a 1-phase mode of operation, the overcurrent setpoint is automatically reduced by half. For overcurrents less than 2.5 times the OCSET level, the over-load condition must exist for 120µs in order to trip the OC fault latch.

For overloads exceeding 2.5 times the set level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection due to hard shorts.

In addition, excessive phase unbalance, for example, due to gate driver failure, will be detected in two-phase operation and the controller will be shut-down after one millisecond's detection of the excessive phase current unbalance. The phase unbalance is detected by the voltage on the ISEN pins if the difference is greater than 9mV.

TABLE 3. FAULT-PROTECTION SUMMARY OF ISL6264

	FAULT DUATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent fault	120µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent fault	<2µs	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Overvoltage fault (1.8V)	immediately	Low-side FET on until Vcore <0.85V, then PWMs three-state, PGOOD latched low (OV-1.8V always)	VDD toggle
Overvoltage fault (+200mV)	1ms	ISL6264 still tries to regulate V_{CORE}, PGOOD latched low	VR_ON toggle or VDD toggle
Undervoltage fault (-300mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle
Unbalance fault (9mV)	1ms	PWM1, PWM2 three-state, PGOOD latched low	VR_ON toggle or VDD toggle

Undervoltage protection is independent of the overcurrent limit. If the output voltage is less than the VID set value by 300mV or more, a fault will latch after one millisecond in that condition. The PWM outputs will turn off and PGOOD will go low. Note that most practical core regulators will have the overcurrent set to trip before the -300mV undervoltage limit.

There are two levels of overvoltage protection and response. For output voltage exceeding the set value by +200mV for 1ms, a fault is declared. All of the above faults have the same action taken except 200mV overvoltage fault: PGOOD is latched low and the upper and lower power FETs are turned off so that inductor current will decay through the FET body diodes. This condition can be reset by bringing VR_ON low or by bringing VDD below 4V. When these inputs are returned to their high operating levels, a soft-start will occur. Under 200mV overvoltage fault, PGOOD is latched low but the ISL6264 still tries to regulate the output voltage.

The second level of overvoltage protection behaves differently. If the output exceeds 1.8V, an OV fault is immediately declared, PGOOD is latched low and the low-side FETs are turned on. The low-side FETs will remain on until the output voltage is pulled down below about 0.85V at which time all FETs are turned off. If the output again rises above 1.7V, the protection process is repeated. This affords the maximum amount of protection against a shorted high-side FET while preventing output ringing below ground. The 1.8V OV is not reset with VR_ON, but requires that VDD be lowered to reset. The 1.8V OV detector is active at all times that the controller is enabled including after one of the other faults occurs so that the processor is protected against high-side FET leakage while the FETs are commanded off.

Offset Voltage

The reference voltage at OFS pin is 1.2V. A resistor (ROFS) connecting the OFS pin to GND will setup a current flowing out of OFS pin. This current is internally mirrored out of FB pin. Therefore, a voltage drop is established across the resistor between FB and VDIFF pin. For the convenience of illustration, name the compensation network resistor between FB and VDIFF as R_{CIN}.

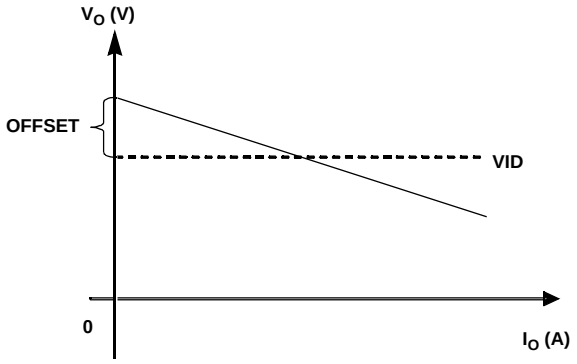


FIGURE 29. LOAD LINE AND OFFSET

$$OFFSET \equiv \frac{1.2V}{R_{OFS}} R_{CIN} \quad \text{(EQ. 1)}$$

Normally we chose RCIN as 1kΩ for the convenience of design, then ROFS of 36.5kΩ will result in a positive OFFSET voltage of 33mV.

Component Selection and Application

Soft-Start and VID Transition Slew Rates

The ISL6264 uses two different slew rates for start-up and the normal operation mode. The first is a slow slew rate in order to reduce inrush current during start-up. Note that the SOFT cap current is bidirectional. The current is flowing into the SOFT capacitor when the output voltage is commanded to rise, and out of the SOFT capacitor when the output voltage is commanded to fall.

The two slew rates are determined by commanding one of two current sources onto the SOFT pin. As can be seen in Figure 30, the SOFT pin has a capacitance to ground. Also, the SOFT pin is the input to the error amplifier and is, therefore, the commanded system voltage. Depending on the state of the system, i.e. Start-Up or After Start-up, one of the two currents shown in Figure 30 will be used to charge or discharge this capacitor, thereby controlling the slew rate of the commanded voltage. These currents can be found under the “Soft-Start Current“ section of theTable Electrical Specifications on page 2.

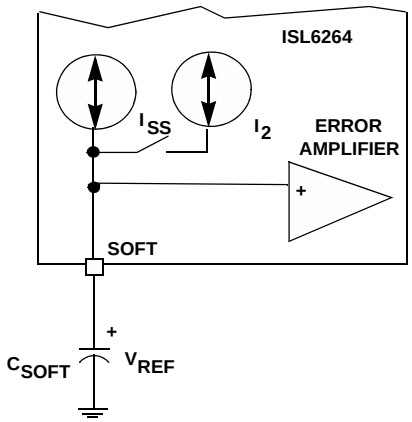


FIGURE 30. SOFT PIN CURRENT SOURCES FOR FAST AND SLOW SLEW RATES

The first current, labelled I_{SS}, is given in the Specification Table as 43A. This current is used during Soft-Start. The second current, I_2 sums with I_{SS} to get the larger of the two currents, labeled IGV in the Electrical Specification Table. This total current is typically 210A with a minimum of 185A.

The symbol, SLEWRATE, will determine the choice of the SOFT capacitor, CSOFT, by Equation 2:

$$C_{SOFT} \equiv \frac{I_2}{SLEWRATE} \quad \text{(EQ. 2)}$$

Using a SLEWRATE of 4.2mV/µs, and the typical I_2 value, given in the Electrical Specification table of 230µA, C_{SOFT} is shown in Equation 3:

$$C_{SOFT} \equiv (230\mu A)/(4.2) \quad \text{(EQ. 3)}$$

A choice of 0.047µF would guarantee a SLEWRATE of 3.7mV/µs is met for minimum I_3 value, given in the Table Electrical Specifications on page 2. This choice of C_{SOFT} will then control the Start-Up slew rate as well. One should expect the output voltage to slew to the VID value of 1.2V at a rate given by Equation 4:

$$\frac{dV}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{43\mu A}{0.047\mu F} = 0.9^{mV}/(\mu S) \quad \text{(EQ. 4)}$$

Selecting R_{BIAS}

To properly bias the ISL6264, a reference current is established by placing a 147kΩ, 1% tolerance resistor from the RBIAS pin to ground. This will provide a highly accurate, 10A current source from which OCSET reference current can be derived.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the R_{BIAS} resistor. Do not connect any other components to this pin as this would negatively impact performance. Capacitance on this pin would create instabilities and should be avoided.

Start-up Operation - PGOOD

The internal timer allows PGOOD to go high approximately 7.6ms after Vout reaches the target VID voltage during the start-up.

Static Mode of Operation - Processor Die Sensing

Die sensing is the ability of the controller to regulate the core output voltage at a remotely sensed point. This allows the voltage regulator to compensate for various resistive drops in the power path and ensure that the voltage seen at the CPU die is the correct level independent of load current.

The VSEN and RTN pins of the ISL6264 are connected to Kelvin sense leads at the die of the processor through the processor socket. These signal names are V_{CC_SENSE} and V_{CC_SENSE} respectively. This allows the voltage regulator to tightly control the processor voltage at the die, independent of layout inconsistencies and voltage drops. This Kelvin sense technique provides for extremely tight load line regulation.

These traces should be laid out as noise sensitive traces. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor must be laid out away from rapidly rising voltage nodes, (switching nodes) and other noisy traces. To achieve optimum performance, place common mode and differential mode capacitor filters to analog ground on VSEN and RTN. Whether to need these capacitors really depends on the actual board layout and noise environment.

Due to the fact that the voltage feedback to the switching regulator is sensed at the processor die, there exists the potential of an over voltage due to an open circuited feedback signal, should the regulator be operated without the processor installed. Due to this fact, we recommend the use of the Ropn1 and Ropn2 connected to V_{OUT} and ground (illustrated in Figure 31). These resistors will provide voltage feedback in the event that the system is powered up without a processor installed. These resistors may typically range from 20Ω to 100Ω.

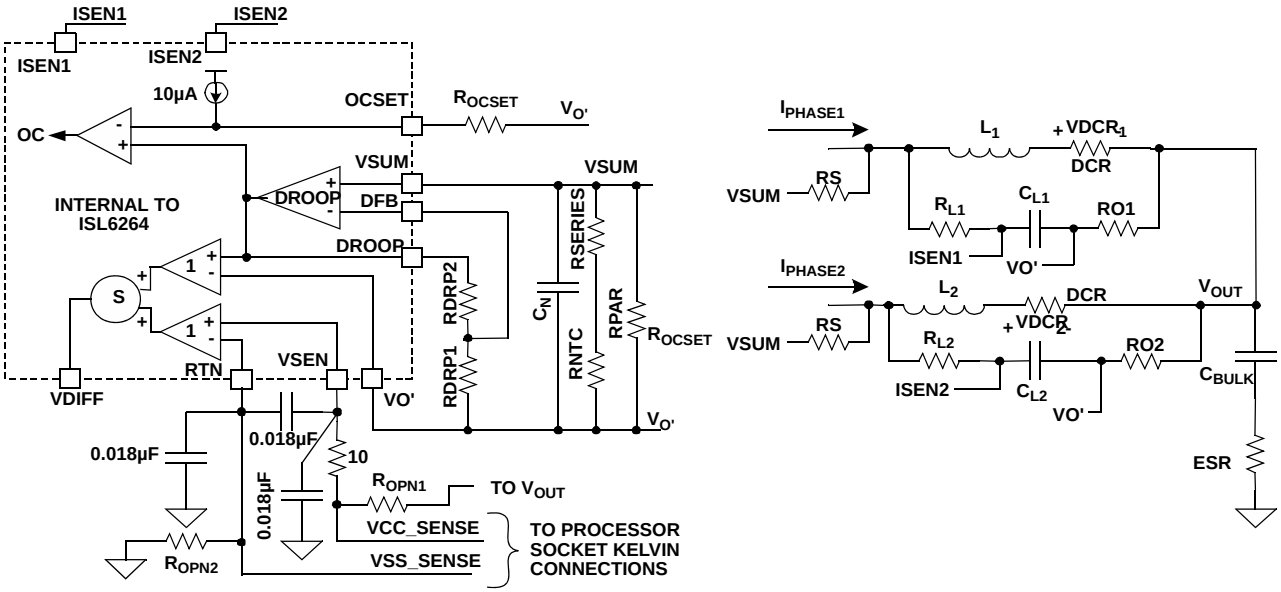


FIGURE 31. SIMPLIFIED SCHEMATIC FOR DROOP AND DIE SENSING WITH INDUCTOR DCR CURRENT SENSING

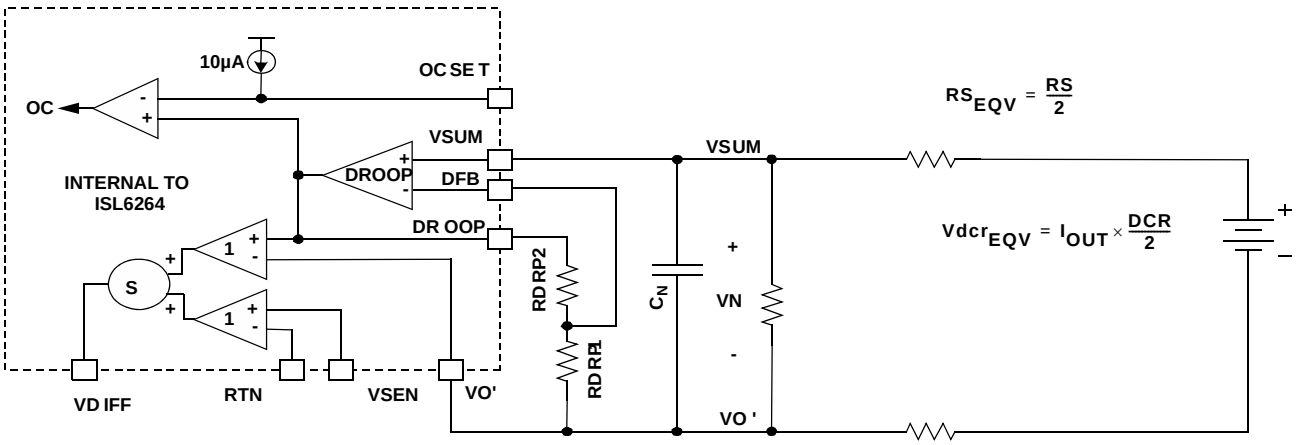


FIGURE 32. SIMPLIFIED SCHEMATIC FOR DROOP AND DIE SENSING WITH INDUCTOR DCR CURRENT SENSING

Setting the Switching Frequency - FSET

The R3 modulator scheme is not a fixed frequency PWM architecture. The switching frequency can increase during the application of a load to improve transient performance.

It also varies slightly due changes in input and output voltage and output current, but this variation is normally less than 10% in continuous conduction mode.

Refer to Figure 2. The resistor connected between the VW and COMP pins of the ISL6264 adjusts the switching window, and therefore adjusts the switching frequency. The RFSET resistor that sets up the switching frequency of the controller operating in CCM can be determined using the following relationship, where RFSET is in kΩ and the switching period is in µs. 6.81kΩ sets about 300kHz switching frequency (see Equation 5).

$$R_{FSET}(k\Omega) \sim (period(\mu s) - 0.4) \cdot 2.33 \quad \text{(EQ. 5)}$$

In discontinuous conduction mode (DCM), the ISL6264 runs into period stretching mode. The switching frequency is dependent on the load current level. In general, the lighter load, the slower switching frequency. Therefore, the switching loss is much reduced for the light load operation, which is important for conserving the battery power in the portable application.

Static Mode of Operation - Static Droop Using DCR Sensing

As previously mentioned, the ISL6264 has an internal differential amplifier which provides very accurate voltage regulation at the die of the processor. The load line regulation is also accurate for both two-phase and single-phase operation. The process of selecting the components for the appropriate load line droop is explained here.

For DCR sensing, the process of compensation for DCR resistance variation to achieve the desired load line droop has several steps and is somewhat iterative.

The two-phase solution using DCR sensing is shown in Figure 31. There are two resistors connecting to the terminals of inductor of each phase. These are labeled RS and R_O. These resistors are used to obtain the DC voltage drop across each inductor. Each inductor will have a certain level of DC current flowing through it, and this current when multiplied by the DCR of the inductor creates a small DC voltage drop across the inductor terminal. When this voltage is summed with the other channels DC voltages, the total DC load current can be derived.

R_O is typically 1Ω to 10Ω. This resistor is used to tie the outputs of all channels together and thus create a summed average of the local CORE voltage output. R_S is determined through an understanding of both the DC and transient load currents. This value will be covered in the next section. However, it is important to keep in mind that the output of each of these R_S resistors are tied together to create the VSUM voltage node. With both the outputs of R_O and R_S tied together, the simplified model for the droop circuit can be derived. This is presented in Figure 32.

Essentially one resistor can replace the R_O resistors of each phase and one R_S resistor can replace the R_S resistors of each phase. The total DCR drop due to load current can be replaced by a DC source, the value of which is given by:

$$V_{DCR\_EQU} = \frac{I_{OUT} \cdot DCR}{2} \quad \text{(EQ. 6)}$$

For the convenience of analysis, the NTC network comprised of R_{ntc}, R_{series} and R_{par}, given in Figure 31, is labelled as a single resistor R_n in Figure 32.

The first step in droop load line compensation is to adjust R_n, R_{OEQV} and R_{SEQV} such that sufficient droop voltage exists even at light loads between the VSUM and VO' nodes. As a rule of thumb we start with the voltage drop across the R_n network, VN, to be 0.5-0.8 times VDCR_EQU. This ratio provides for a fairly reasonable amount of light load signal from which to arrive at droop.

The resultant NTC network resistor value is dependent on the temperature and given by Equation 7:

$$R_n(T) = \frac{(R_{series} + R_{ntc}) \cdot R_{par}}{R_{series} + R_{ntc} + R_{par}} \quad \text{(EQ. 7)}$$

For simplicity, the gain of V_N to the V_{DCR_EQU} is defined by G1, also dependent on the temperature of the NTC thermistor (see Equation 8).

$$G_1(T) = \frac{R_n(T)}{R_n(T) + R_{sequ}} \quad \text{(EQ. 8)}$$

$$DCR(T) = DCR_{25C} \cdot (1 + 0.00393*(T\text{-}25)) \quad \text{(EQ. 9)}$$

Therefore, the output of the droop amplifier divided by the total load current can be expressed in Equation 10:

$$R_{droop} = G_1(T) \cdot \frac{DCR_{25}}{2} \cdot (1 + 0.00393*(T\text{-}25)) \cdot k_{droop} \quad \text{(EQ. 10)}$$

where R_{DROOP} is the realized load line slope and 0.00393 is the temperature coefficient of the copper. To achieve the droop value independent from the temperature of the inductor, it is equivalently expressed by Equation 11:

$$G_1(T) \cdot (1 + 0.00393*(T\text{-}25)) \cong G_{1target} \quad \text{(EQ. 11)}$$

The non-inverting droop amplifier circuit has the gain $k_{droopamp}$ expressed as shown in Equation 12:

$$k_{droopamp} = 1 + \frac{R_{drp2}}{R_{drp1}} \quad \text{(EQ. 12)}$$

$G_{1target}$ is the desired gain of Vn over I_{OUT}. DCR/2. Therefore, the temperature characteristics of gain of Vn is described in Equation 13:

$$G_1(T) = \frac{1_{1target}}{(1 + 0.00393*(T\text{-}25))} \quad \text{(EQ. 13)}$$

For the G1 target = 0.76, the R_{ntc} = 10kΩ with b = 4300, R_{series} = 2610kΩ, and R_{par} = 11kΩ, R_{seqv} = 1825Ω generates a desired G1, close to the feature specified in Equation 20. The actual G1 at +25°C is 0.769. For different G1 and NTC thermistor preference, the design file to generate the proper value of R_{ntc}, R_{series}, R_{par}, and R_{seqv} is provided by Intersil.

Then, the individual resistors from each phase to the VSUM node, labeled R_{S1} and R_{S2} in Figure 31, are then given by Equation 14.

$$Rs = 2 \cdot R_{seqv} \quad \text{(EQ. 14)}$$

So, R_S = 3650Ω. Once we know the attenuation of the R_S and R_n network, we can then determine the droop amplifier gain required to achieve the load line. Setting Rdrp1 = 1k_1%, then Rdrp2 is can be found using Equation 15:

$$R_{drp2} = \left(\frac{2 \cdot R_{droop}}{DCR \cdot G1(25°C)} - 1\right) \cdot R_{drp1} \quad \text{(EQ. 15)}$$

Droop Impedance (R_{DROOP}) = 0.002 (V/A) as per the AMD specification, DCR = 0.0008Ω typical for a 0.36µH inductor, Rdrp1 = 1kΩ and the attenuation gain (G1) = 0.77, Rdrp2 is then:

$$R_{drp2} = \left(\frac{2 \cdot R_{droop}}{0.0008 \cdot 0.769} - 1\right) \cdot 1k\Omega = 5.62k\Omega \quad \text{(EQ. 16)}$$

Note, we choose to ignore the R_O resistors because they do not add significant error.

These designed values in R_n network are very sensitive to layout and coupling factor of the NTC to the inductor. As only one NTC is required in this application, this NTC should be placed as close to the Channel 1 inductor as possible and PCB traces sensing the inductor voltage should be go directly to the inductor pads.

Once the board has been laid out, some adjustments may be required to adjust the full load droop voltage. This is fairly easy and can be accomplished by allowing the system to achieve thermal equilibrium at full load, and then adjusting Rdrp2 to obtain the appropriate load line slope.

To see whether the NTC has compensated the temperature change of the DCR, the user can apply full load current and wait for the thermal steady state and see how much the output voltage will deviate from the initial voltage reading. A good compensation can limit the drift to 2mV. If the output voltage is decreasing with temperature increase, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. The user should follow the evaluation board value and layout of NTC as much as possible to minimize engineering time.

The 2mV/A load line should be adjusted by Rdrp2 based on maximum current, not based on small current steps like 10A, as the droop gain might vary between each 10A steps. Basically, if the max current is 40A, the required droop voltage is 84mV. The user should have 40A load current on and look for 84mV droop. If the drop voltage is less than 84mV, for example, 80mV. the new value will be calculated by:

$$R_{drp2} = \frac{84mV}{80mV}(R_{drp1} + R_{drp2}) - R_{drp1} \quad \text{(EQ. 17)}$$

Do not let the mismatch get larger than 600Ω. To reduce the mismatch, multiply both R_{drp1} and R_{drp2} by the appropriate factor. The appropriate factor in the example is 1404/853 = 1.65. In summary, the predicted load line with the designed droop network parameters based on the design tool is shown in Figure 33.

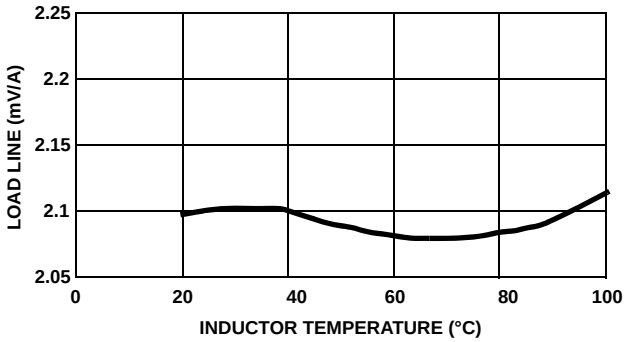


FIGURE 33. LOAD LINE PERFORMANCE WITH NTC THERMAL COMPENSATION

Dynamic Mode of Operation - Dynamic Droop Using DCR Sensing

Droop is very important for load transient performance. If the system is not compensated correctly, the output voltage could sag excessively upon load application and potentially create a system failure. The output voltage could also take a long period of time to settle to its final value. This could be problematic if a load dump were to occur during this time. This situation would cause the output voltage to rise above the no load setpoint of the controller and could potentially damage the CPU.

The L/DCR time constant of the inductor must be matched to the Rn*C_n time constant as shown in Equation 18:

$$\frac{L}{DCR} = \frac{R_n \cdot RS_{EQV}}{R_n + RS_{EQV}} \cdot C_n \quad \text{(EQ. 18)}$$

Solving for C_n, we now have Equation 19:

$$C_n = \frac{\frac{L}{DCR}}{\frac{R_n \cdot RS_{EQV}}{R_n + RS_{EQV}}} \quad \text{(EQ. 19)}$$

Note, R_O was neglected. As long as the inductor time constant matches the C_n, R_n and R_S time constants as given above, the transient performance will be optimum. As in the Static Droop Case, this process may require a slight adjustment to correct for layout inconsistencies. For the example of L = 0.36 H with 0.8mΩ DCR, C_n is calculated as shown in Equation 20:

$$C_n = \frac{\frac{0.36\mu H}{0.0008}}{\text{parallel}(5.823k, 1.825k)} = 330nF \quad \text{(EQ. 20)}$$

The value of this capacitor is selected to be 330nF. As the inductors tend to have 20% to 30% tolerances, this cap generally will be tuned on the board by examining the transient voltage. If the output voltage transient has an initial dip (lower than the voltage required by the load line) and slowly increases back to the steady state, the cap is too small and vice versa. It is better to have the cap value a little bigger to cover the tolerance of the inductor to prevent the output voltage from going lower than the spec. This cap needs to be a high grade cap like X7R with low tolerance. There is another consideration in order to achieve better time constant match mentioned above. The NPO/COG (class-I) capacitors have only 5% tolerance and a very good thermal characteristics. But those caps are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier has to be resized up to 10X to reduce the capacitance by 10X. But attention has to be paid in balancing the impedance of droop amplifier in this case.

Dynamic Mode of Operation - Compensation Parameters

Considering the voltage regulator as a black box with a voltage source controlled by VID and a series impedance, in order to achieve the 2.0mV/A load line, the impedance needs to be 2.0mΩ. The compensation design has to target the output impedance of the controller to be 2.0mΩ. There is a mathematical calculation file available to the user. The power stage parameters such as L and C_S are needed as the input to calculate the compensation component values. Attention has to be paid to the input resistor to the FB pin. It is better to keep this resistor at 1kΩ for the convenience of OFFSET design.

Static Mode of Operation - Current Balance Using DCR or Discrete Resistor Current Sensing

Current Balance is achieved in the ISL6264 through the matching of the voltages present on the ISEN pins. The ISL6264 adjusts the duty cycles of each phase to maintain equal potentials on the ISEN pins. RL and CL around each inductor, or around each discrete current resistor, are used to create a rather large time constant such that the ISEN voltages have minimal ripple voltage and represent the DC current flowing through each channel's inductor. For optimum performance, RL is chosen to be 10kΩ and CL is selected to be 0.22µF. When discrete resistor sensing is used, a capacitor most likely needs to be placed in parallel with RL to properly compensate the current balance circuit.

ISL6264 uses RC filter to sense the average voltage on phase node and forces the average voltage on the phase node to be equal for current balance. Even though the ISL6264 forces the ISEN voltages to be almost equal, the inductor currents will not be exactly equal. Take DCR current sensing as example, two errors have to be added to find the total current imbalance.

1. Mismatch of DCR: If the DCR has a 5% tolerance then the resistors could mismatch by 10% worst case. If each phase is carrying 20A then the phase currents mismatch by 20A*10% = 2A.
2. Mismatch of phase voltages/offset voltage of ISEN pins. The phase voltages are within 2mV of each other by current balance circuit. The error current that results is given by 2mV/DCR. If DCR = 1mΩ then the error is 2A.

In the above example, the two errors add to 4A. For the two phase DC/DC, the currents would be 22A in one phase and 18A in the other phase. In the above analysis, the current balance can be calculated with 2A/20A = 10%. This is the worst case calculation, for example, the actual tolerance of two 10% DCRs is 10%*sqrt(2) = 7%.

Fault Protection - Overcurrent Fault Setting

As previously described, the Overcurrent protection of the ISL6264 is related to the Droop voltage. Previously we have calculated that the Droop Voltage = ILoad * R_{droop}, where R_{droop} is the load line slope specified as 2mV/A in the AMD specification. Knowing this relationship, the over current protection threshold can be set up as a voltage Droop level. Knowing this voltage droop level, one can program in the appropriate drop across the R_{oc} resistor. This voltage drop will be referred to as V_{oc}. Once the droop voltage is greater than V_{oc}, the PWM drives will turn off and PGOOD will go low.

The selection of R_{oc} is given in Equation 21. Assuming we desire an overcurrent trip level (Ioc) of 55A, and knowing from the Intel Specification that the load line slope (R_{droop}) is 0.0021 (V/A), we can then calculate for R_{oc} as shown in Equation 21.

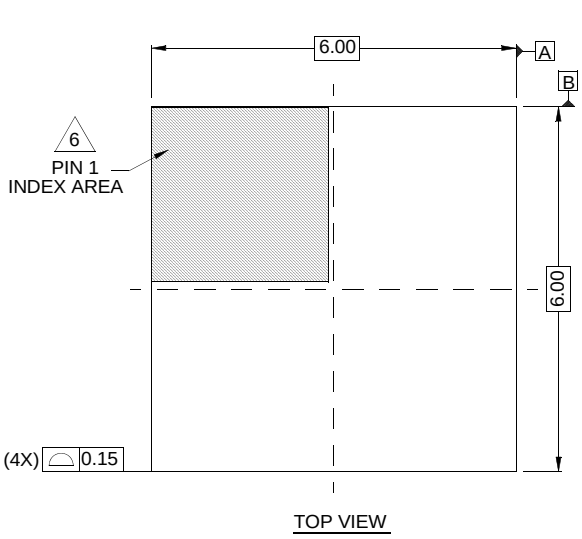
$$R_{OC} = \frac{I_{OC} \cdot R_{droop}}{10\mu A} = \frac{55 \cdot 0.002}{10 \cdot 10^{-6}} = 11.5k\Omega \qquad \text{(EQ. 21)}$$

Note, if the droop load line slope is not -0.002 (V/A) in the application, the over current setpoint will differ from predicted.

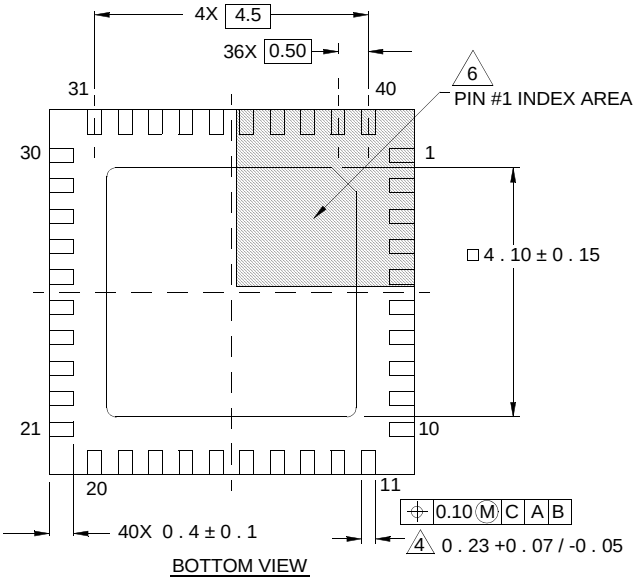
Package Outline Drawing

L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 10/06



TOP VIEW



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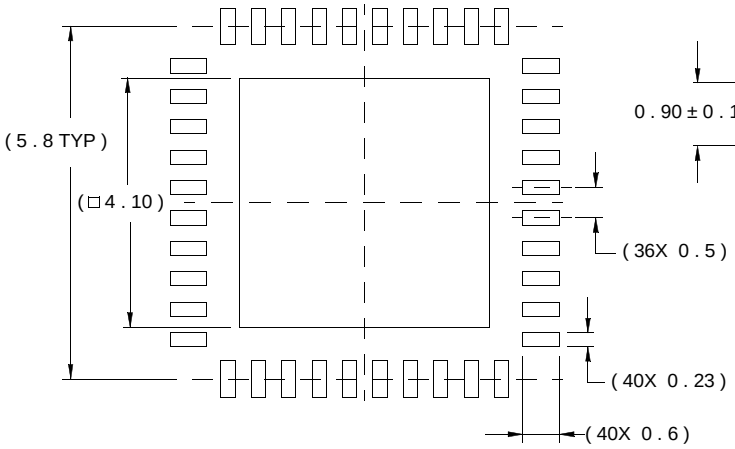
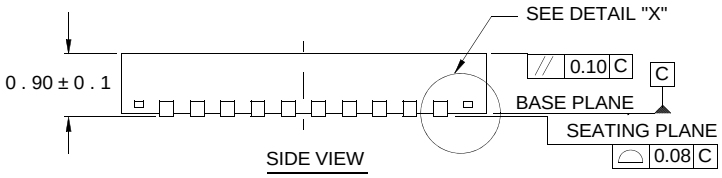
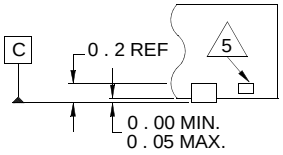


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.